

DESCRIPTION

PT2308L is a Class AB stereo headphone driver chip utilizing CMOS Technology specially designed for portable digital audio applications. It is housed in an 8-pin DIP or SOP package and is functionally compatible with TDA1308. Pin assignments and application circuit are optimized for lower cost effectiveness and easy PCB Layout.

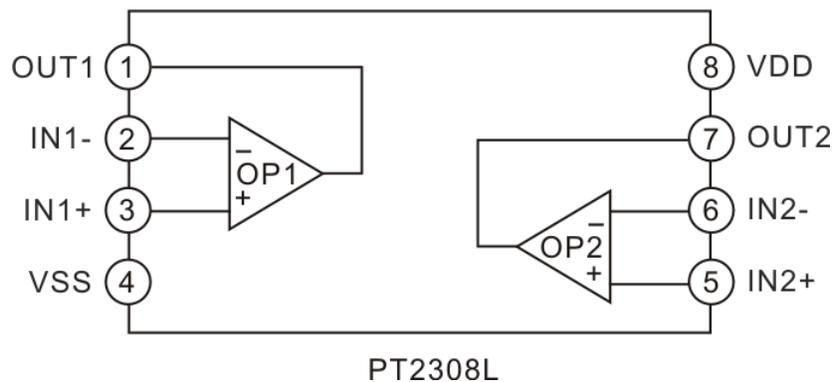
FEATURES

- CMOS technology
- Low power consumption
- Wide temperature range
- Excellent power supply ripple rejection
- High signal-to-noise ratio, S/N=110dB
- Low harmonic distortion, THD= 0.001%
- Large output voltage swing
- Low supply voltage available (VDD=2V)

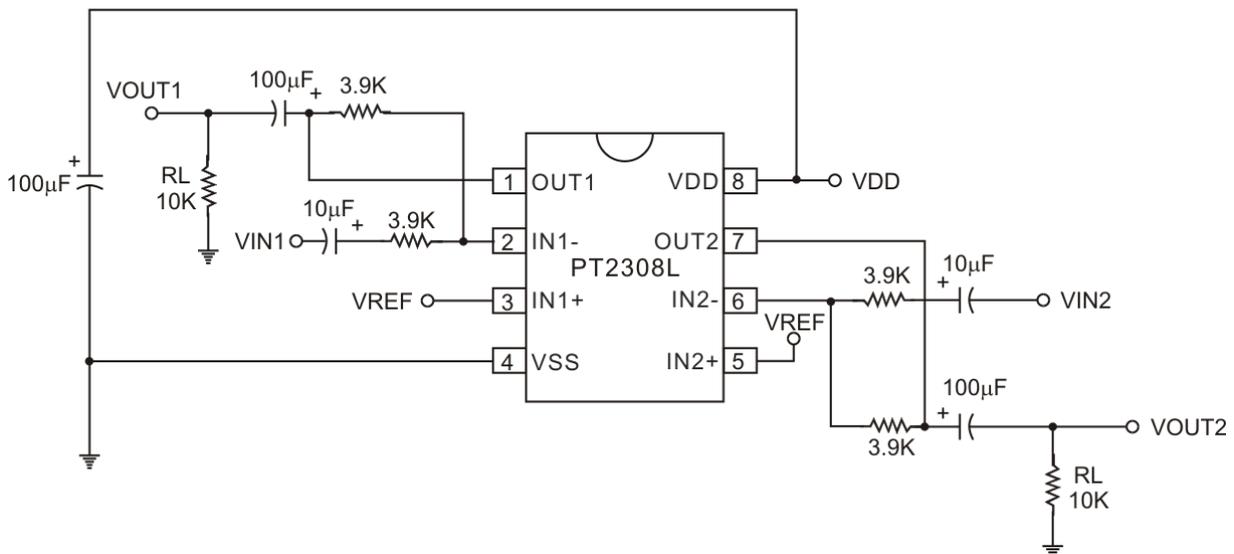
APPLICATIONS

- Portable digital audio
- Hi-Fi audio system
- Walkman
- CD-ROM

BLOCK DIAGRAM



APPLICATION CIRCUIT

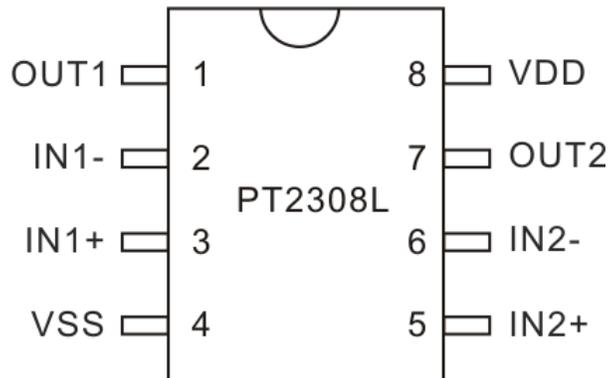


Note: VREF=1/2 VDD

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2308L	8 Pins, DIP, 300mil	PT2308L
PT2308L-S	8 Pins, SOP, 150mil	PT2308L-S

PIN CONFIGURATION



PIN DESCRIPTION

Symbol	I/O	Description	Pin No.
OUT1	O	Output pin 1	1
IN1-	I	Inverting input pin 1	2
IN1+	I	Non-inverting input pin 1	3
VSS	-	Negative power supply	4
IN2+	I	Non-inverting input pin 2	5
IN2-	I	Inverting input pin 2	6
OUT2	O	Output pin 2	7
VDD	-	Positive power supply	8

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Supply voltage	VDD	8	V
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-65 to +150	°C

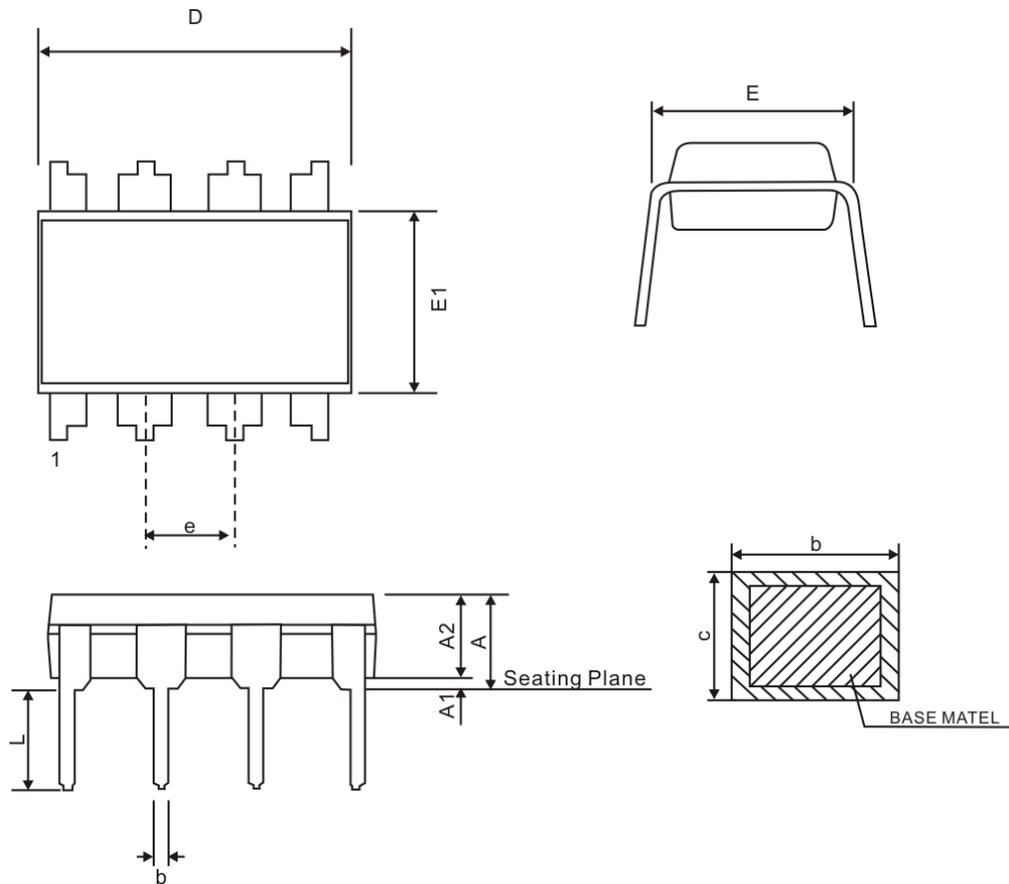
ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, VDD=3V, VSS=0V, Ta=25°C, fin=1KHz, RL=32Ω)

Parameter	Symbol	Conditions	Min	Typ.	Max.	Unit	
Single power supply	VDD		2	3	4	V	
Dual power supply			+1.0	+1.5	+2.0		
Single power supply	VSS		0	0	0	V	
Dual power supply			-1.0	-1.5	-2.0		
Supply current	IDD	No Load, VDD=3V	-	7	-	mA	
Total power dissipation	Ptot	No Load, VDD=3V	-	21	-	mW	
Max. output power (RL=32Ω)	Po	THD=0.15%	VDD=1.8V	-	5.8	-	mW
			VDD=3V	-	23	-	
		THD=3%	VDD=1.8V	-	8.2	-	
			VDD=3V	-	27	-	
Total harmonic distortion	THD	Vo(p-p)=2V	-	0.03	0.06	%	
		Vo(p-p)=2V, (RL=5KΩ)	-	0.001	-		
Signal to noise ratio	S/N	A-weighted	100	110	-	dB	
Channel separation	acs	RL=32Ω	-	105	-	dB	
		RL=5KΩ	-	100	-		
Power supply ripple rejection	PSRR	fin=100Hz Vripple(p-p)=100mV	-	90	-	dB	
Output impedance	Ro	Gain=0dB	-	1	-	Ω	
Slew rate	SR	Gain=0dB inverting	-	3.5	-	V/μs	

PACKAGE INFORMATION

8 PINS, DIP, 300MIL

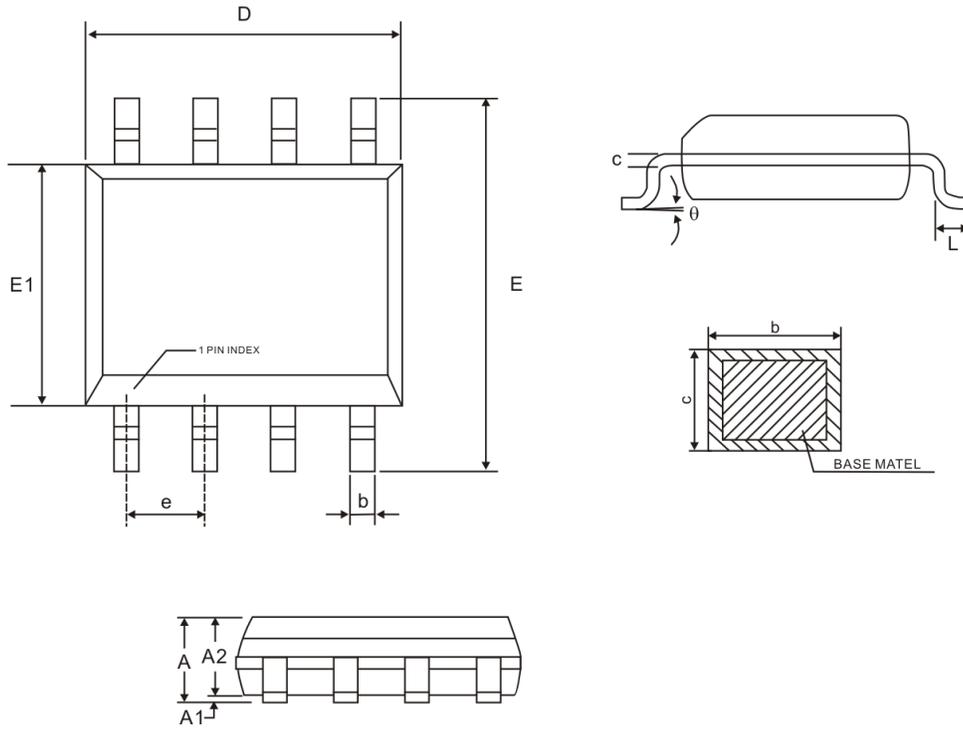


Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	4.80
A1	0.50	-	-
A2	3.10	3.30	3.50
b	0.38	-	0.55
c	0.21	-	0.35
D	9.10	9.20	9.30
E	7.62	7.87	8.25
E1	6.25	6.35	6.45
e	2.54BSC		
L	2.92	3.30	3.81

Notes:

1. Refer to JEDEC MS-001, Variation BA
2. All dimensions are in millimeter

8 PINS, SOP, 150MIL



Symbol	Millimeter		
	Min.	Nom.	Max.
A	1.35	1.60	1.77
A1	0.08	0.15	0.28
A2	1.20	1.40	1.65
b	0.33	-	0.51
c	0.17	-	0.26
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.38	0.60	1.27
θ	0°	-	8°

- Notes:
1. Refer to JEDEC MS-012AA
 2. All dimensions are in millimeter

IMPORTANT NOTICE

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