# PT2369
## 4 Inputs, 2.6Wx2 Class-AB Audio Amplifier with I²C Volume

## DESCRIPTION

The PT2369 is an audio amplifier design for the low voltage (5V) application purpose, built-in stereo 2.6W Class-AB power amplifier with 32 steps I²C controlled volume, it also provides 4 sources selector, and unique noise suppressor circuit eliminates unpleasant pop noise during power or shutdown on/off, and provides SE/BTL selection for headphone connection.

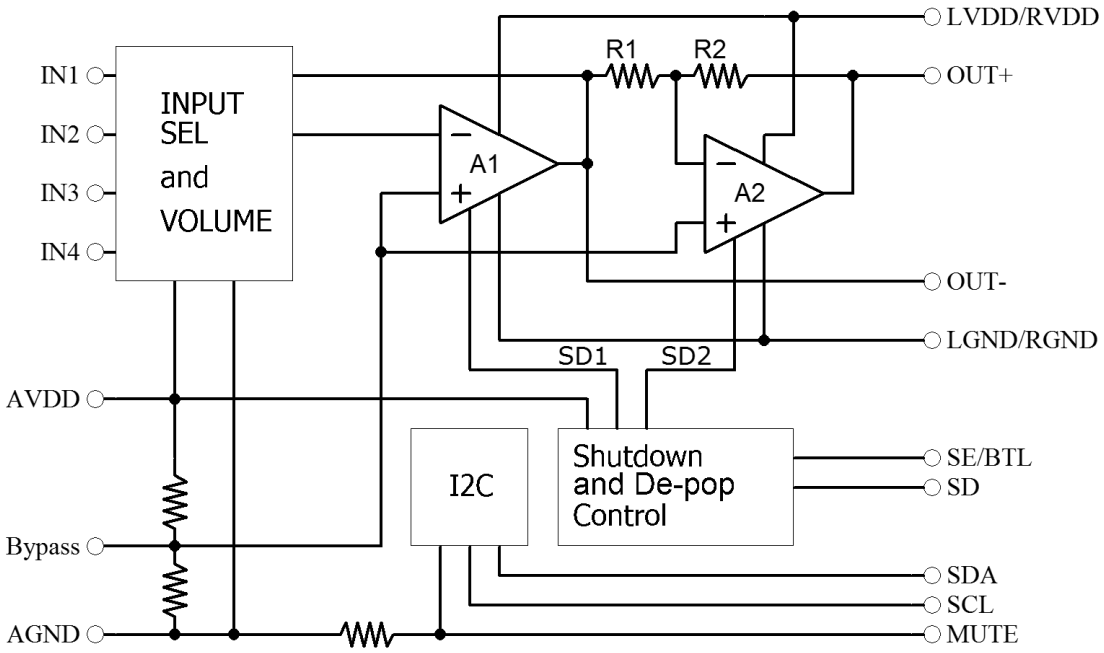
## APPLICATIONS

- Portable DVD player
- Portable audio system
- Docking speaker system
- Flat panel monitor
- Other audio applications

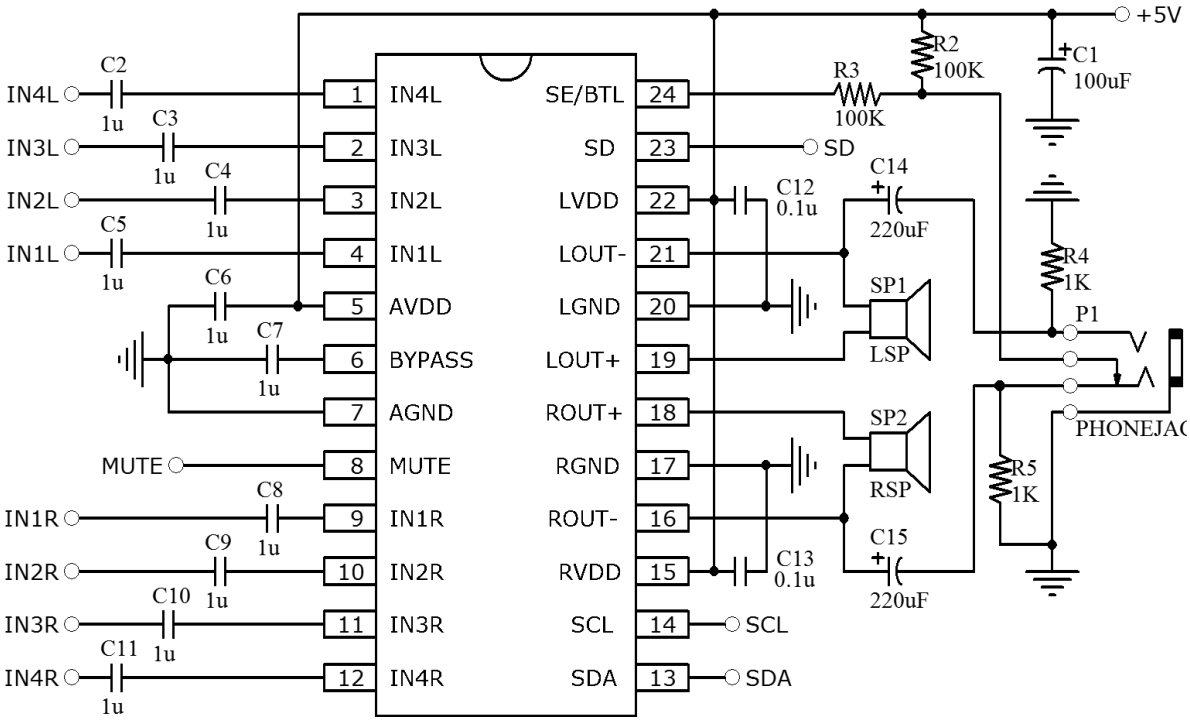
## FEATURES

- Supply voltage: 3~6V
- 4 Stereo inputs
- 32 steps, I²C controlled volume from -40dB to +26dB (BTL)
- 2.6W x 2 Class-AB Power Amplifier (VDD=5V, RL=4Ω, THD=10%)
- BTL and SE output selectable
- Pop-Free circuitry eliminates unpleasant noises during power ON/OFF and changing the input source.
- Low power shutdown
- Over Temperature Protection
- Over Current Protection
- TSSOP 24 pin package with thermal pad

## BLOCK DIAGRAM



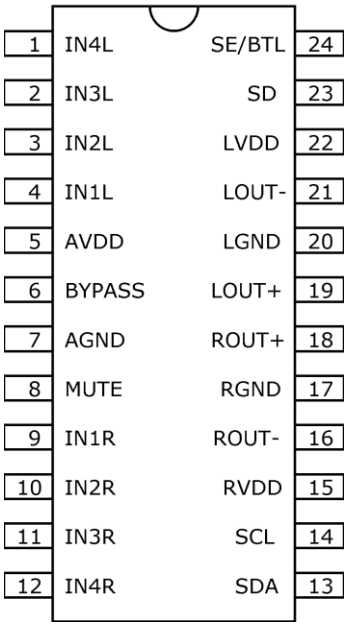
# APPLICATION CIRCUIT




# ORDER INFORMATION

| Part Number | Package Type | Top Code |
|---|---|---|
| PT2369-HT | 24 pins, HTSSOP, 173mil | PT2369-HT |

# PIN CONFIGURATION




# PIN DESCRIPTION

| Pin Name | I/O | Description | Pin No. |
|---|---|---|---|
| IN4L | I | Left channel positive input 4 | 1 |
| IN3L | I | Left channel positive input 3 | 2 |
| IN2L | I | Left channel positive input 2 | 3 |
| IN1L | I | Left channel positive input 1 | 4 |
| AVDD | P | Power input for volume control | 5 |
| BYPASS | I | Internal 1/2 reference bypassing | 6 |
| AGND | P | Ground for volume control | 7 |
| MUTE | I | Mute Input, H=muted, L=normal (internal pull down) | 8 |
| IN1R | I | Right channel positive input 1 | 9 |
| IN2R | I | Right channel positive input 2 | 10 |
| IN3R | I | Right channel positive input 3 | 11 |
| IN4R | I | Right channel positive input 4 | 12 |
| SDA | I | I2C data input | 13 |
| SCL | I | I2C clock input | 14 |
| RVDD | I | Right channel power input | 15 |
| ROUT- | O | Right channel negative output | 16 |
| RGND | P | Power GND | 17 |
| ROUT+ | O | Right channel positive output | 18 |
| LOUT+ | O | Left channel positive output | 19 |
| LGND | P | Power GND | 20 |
| LOUT- | O | Left channel negative output | 21 |
| LVDD | P | Left channel power input | 22 |
| SD | I | Shutdown, L=shutdown, H=normal operate. | 23 |
| SE/BTL | I | L=BTL (speaker out), H=SE (Headphone out) | 24 |

# FUNCTION DESCRIPTION

## *INPUT SELECTOR AND VOLUME*

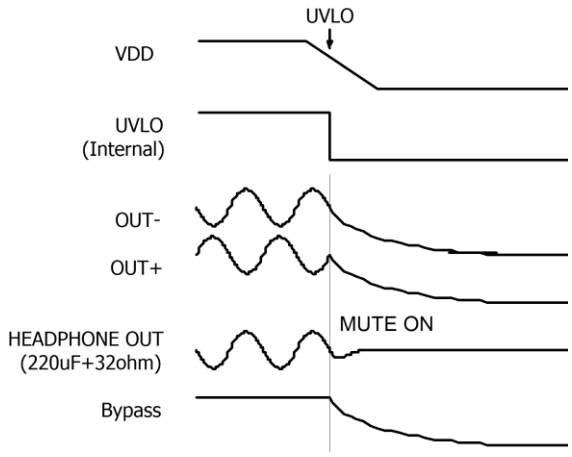
The PT2369 provides 4 stereo inputs selector; all of input pin should be AC coupled. Please note the input impedance is relative with volume setting, higher gain means lower input impedance, the minimum input impedance is around 18KΩ at the +26dB gain setting. In a general application, a 1μF capacitor is recommended for enough low frequency responses. All of volume and input selector setting is via $I^2C$ bus command; please refer to the software control section.

## *DE-POP AND MUTE*

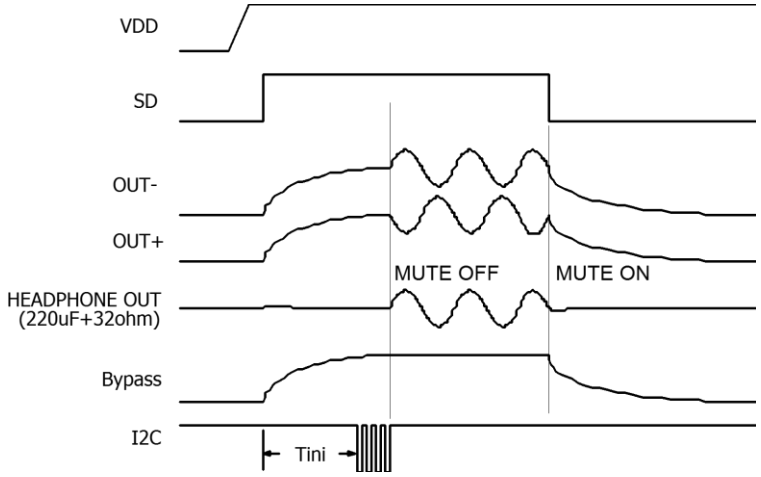
The PT2369 has internal de-pop mechanism for all of conditions, whatever in shutdown ON-OFF or power ON-OFF period. A voltage sensing circuit would monitor the bias, reference and VDD relations continuously to avoid pop noise happens, and volume controller default sets to mute-on to avoid any audible output, therefore, user must given a initial setting to the PT2369 after power-on period. If supply voltage was removed suddenly, the UVLO circuit will detects such changes and mute all of amplifier immediately to prevent pop noises.

After power-on period, the I2C bus needs a short waiting time (Tini) to send the initial setting into $I^2C$ register. The Tini timing determinate by Cbypass capacitance, it is must waiting the Bypass voltage exceeds 0.3VDD to prevent initializing failed.

The PT2369 has hardware mute and software mute could choose for general use, both mute signal is combine together in the internal circuit, whatever which was actives the outputs will be muted.




Power-Off mute timing




Shutdown ON-OFF mute timing

## POWER AMPLIFIER

The power amplifier can driving up to 2.6W into 4Ω load and output configuration can be selected between BTL and single ended (SE) for different type load; a low impedance loudspeaker or a 32Ω headphone. The SE/BTL pin is determinate which mode activated; please refer to the application circuit for proper connection. To protect the amplifier output stage not be damaged by unusual short circuit, the maximum output current is limited by not exceeds 2.5A.

## SHUTDOWN

The shutdown function could eliminate all of current consumption, pull the SD pin down to GND and whole chip current consumption will drop down to less than 1μA even the VDD still powered. When shutdown is active, the amplifier would be turn-off immediately and all of internal register will reminds original setting if the VDD is not removed. Sets the SD pin to high can turn-on the chip, de-pop circuit will associate in same time to avoid pop noise generated.

## THERMAL PROTECTION

If chip is not well soldered on a board with broad copper foil, or operating ambient temperature exceeds thermal derating limit, the chip's junction temperature will exceeds 150℃ and causes permanent damage. The thermal protection circuit will be activated when junction temperature exceed 150℃ to prevent long-time overheat damages. When thermal protection is activated the output will be temporary turn off for cooling down, and it will back to normal operation when junction temperature below 100℃.

## SYSTEM RESET

A Power-On-Reset signals will reset all of registers to default value if the supply voltage is drop down to zero then rising up to exceeds 1.5V. After power-on-reset sequence user should given all of registers a validate value to ensure whole chip work properly.

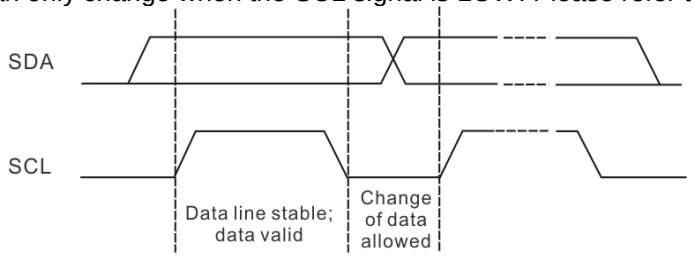
# CONTROL BUS SPECIFICATION

## *BUS INTERFACE*

All functions of the PT2369 are controlled by the $I^2C$ interface, the interface is consisting by SDA and SCL pins. Detail protocol of the $I^2C$ bus will discuss on the next section. It should be noted that the bus level pull-up resistors connected to the PT2369 positive supply voltage may required in some application especially the MCU output high level is no enough.

## *DATA VALIDITY*

A data on the SDA Line is considered valid and stable only when the SCL Signal is in HIGH State. The HIGH and LOW State of the SDA Line can only change when the SCL signal is LOW. Please refer to the figure below.



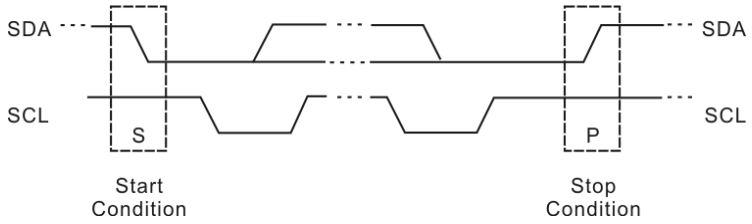

## *START AND STOP CONDITIONS*

A Start Condition is activated when

1) The SCL is set to HIGH and
2) SDA shifts from HIGH to LOW State.

The Stop Condition is activated when

1) SCL is set to HIGH and
2) SDA shifts from LOW to HIGH State. Please refer to the timing diagram below.

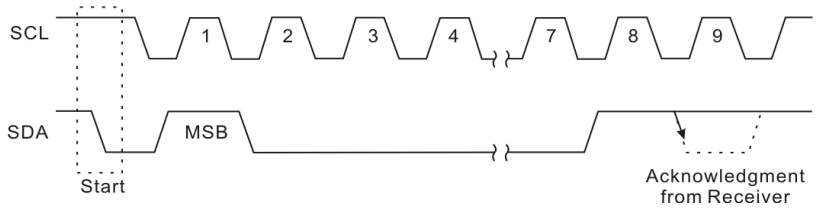



## *BYTE FORMAT*

Every byte transmitted to the SDA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is first transmitted.

## ACKNOWLEDGE

During the Acknowledge clock pulse (ACK), the SDA output port of the master device (μP) would be sets on Hi-Z state, if peripheral device (ex : audio processor) recognize the I²C command the SDA line will be pull-down by slave device during the SCL clock pulse held in HIGH state period. Please refer to the diagram below. The slave device that has been addressed to generate an Acknowledge after receiving each byte, otherwise, the SDA Line will remain at the High level in period of the ninth (9th) clock pulse. In this case, the host controller will generate a STOP sign in order to abort the transfer mission.




## TRANSMISSION WITHOUT ACKNOWLEDGE

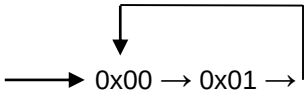
If the application does not need to verify the Acknowledge signal that generated by the slave device is right or not, host controller can just bypass the acknowledge check and transmit next data byte to the slave device. If this approach is used, there are greater chances of faulty operation as well as decrease in noise immunity.

## I²C BUS FORMAT

| S | Slave Address | A | Sub Address | A | Data Bits | A | P |
|---|---|---|---|---|---|---|---|

S: Starting Term
A: Acknowledge Bit
P: Stop Term

After the Data bits was written into the Data register, the Sub Address register will automatic point to next new Sub Address, therefore, user only need to send first Sub Address only and DATA bits can transmit continuously, does not need appoint a new Sub Address again. Next graph shows the Sub Address increasing sequence.




## SLAVE ADDRESS

The PT2369 sub address is fixed on 0x86.

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

## SUB ADDRESS TABLE

| Sub Address | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0x00 | AIN1 | AIN0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x01 | VOL4 | VOL3 | VOL2 | VOL1 | VOL0 | 0 | 0 | MUTE |

# *DATA BYTE DEFINITION*

## <1> MUTE (SUB ADDRESS 0X01)

| Mute | Data Bit |
|---|---|
| | D0 |
| | AMUTE |
| Mute on | 0* |
| Normal | 1 |

## <2> AUDIO INPUT SELECTOR (SUB ADDRESS 0X00)

| Input SEL | Data Bit | |
|---|---|---|
| | D7 | D6 |
| | AIN1 | AIN0 |
| IN1 | 0* | 0* |
| IN2 | 0 | 1 |
| IN3 | 1 | 0 |
| IN4 | 1 | 1 |

*=Default value

## <3> VOLUME CONTROL (SUB ADDRESS 0X01)

| Volume Gain (dB) | | Sub Address | Data Bit | | | | |
|---|---|---|---|---|---|---|---|
| | | | D7 | D6 | D5 | D4 | D3 |
| BTL | SE | 0x01 | VOL4 | VOL3 | VOL2 | VOL1 | VOL0 |
| +26 | +20 | | 0 | 0 | 0 | 0 | 0 |
| +25 | +19 | | 0 | 0 | 0 | 0 | 1 |
| +24 | +18 | | 0 | 0 | 0 | 1 | 0 |
| +23 | +17 | | 0 | 0 | 0 | 1 | 1 |
| +22 | +16 | | 0 | 0 | 1 | 0 | 0 |
| +20 | +14 | | 0 | 0 | 1 | 0 | 1 |
| +18 | +12 | | 0 | 0 | 1 | 1 | 0 |
| +16 | +10 | | 0 | 0 | 1 | 1 | 1 |
| +14 | +8 | | 0 | 1 | 0 | 0 | 0 |
| +12 | +6 | | 0 | 1 | 0 | 0 | 1 |
| +10 | +4 | | 0 | 1 | 0 | 1 | 0 |
| +8 | +2 | | 0 | 1 | 0 | 1 | 1 |
| +6 | 0 | | 0 | 1 | 1 | 0 | 0 |
| +4 | -2 | | 0 | 1 | 1 | 0 | 1 |
| +2 | -4 | | 0 | 1 | 1 | 1 | 0 |
| 0 | -6 | | 0 | 1 | 1 | 1 | 1 |
| -2 | -8 | | 1 | 0 | 0 | 0 | 0 |
| -4 | -10 | | 1 | 0 | 0 | 0 | 1 |
| -6 | -12 | | 1 | 0 | 0 | 1 | 0 |
| -8 | -14 | | 1 | 0 | 0 | 1 | 1 |
| -10 | -16 | | 1 | 0 | 1 | 0 | 0 |
| -12 | -18 | | 1 | 0 | 1 | 0 | 1 |
| -14 | -20 | | 1 | 0 | 1 | 1 | 0 |
| -16 | -22 | | 1 | 0 | 1 | 1 | 1 |
| -18 | -24 | | 1 | 1 | 0 | 0 | 0 |
| -20 | -26 | | 1 | 1 | 0 | 0 | 1 |
| -22 | -28 | | 1 | 1 | 0 | 1 | 0 |
| -24 | -30 | | 1 | 1 | 0 | 1 | 1 |
| -28 | -34 | | 1 | 1 | 1 | 0 | 0 |
| -32 | -38 | | 1 | 1 | 1 | 0 | 1 |
| -36 | -42 | | 1 | 1 | 1 | 1 | 0 |
| -40 | -46 | | 1* | 1* | 1* | 1* | 1* |

*=Default value

# ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply Voltage | VDD | 0 | 7 | V |
| Operating Temperature | Topr | -45 | 85 | ℃ |
| Storage Temperature | Tstg | -65 | 150 | ℃ |
| Maximum Input Voltage | Vi max | -0.3 | VDD+0.3 | V |
| ESD | HBM | -2 | +2 | KV |
| | MM | -200 | +200 | V |
| I/O Latch Up | $I_{LU}$ | -150 | +150 | mA |

# ELECTRICAL CHARACTERISTICS

Unless stated otherwise: VDD=5V, Test bandwidth=22~22KHz

| Parameter | Symbol | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| ***POWER SUPPLY*** | | | | | | | |
| Supply Voltage | VDD | | | 3 | 5 | 6 | V |
| Supply Current | IDD | SE | VDD=3V | - | 5 | 9 | mA |
| | | | VDD=5V | - | 6 | 11 | |
| | | BTL | VDD=3V | - | 8 | 12 | |
| | | | VDD=5V | - | 10 | 15 | |
| | | SD=1V | | - | - | 1 | μA |
| Under Voltage Lock Out | UVLO | Output ON | | - | 3 | - | V |
| | | Output Off | | - | 2.7 | - | |
| ***INPUT SELECTOR AND VOLUME*** | | | | | | | |
| **Input Selector** | | | | | | | |
| Input Isolation | SIN | F=1KHz | | - | 90 | - | dB |
| Input Resistance | Rin | VOL=-40dB | | - | 200 | - | KΩ |
| | | VOL=+26dB | | - | 20 | - | |
| | | Inputs not selected | | - | 50 | - | |
| **Volume Control** | | | | | | | |
| Maximum Gain | Gmax | BTL(code=00000) | | - | 26 | - | dB |
| Minimum Gain | Gmin | BTL(code=11111) | | - | -40 | - | dB |
| Volume Step | $G_{STEP}$ | Vol=+26~+22dB | | - | 1 | - | dB |
| | | Vol=+20~-24dB | | - | 2 | - | |
| | | Vol=-28~-40dB | | - | 4 | - | |
| Attenuation Error | $E_A$ | Vol=+26~-40dB | | -1 | 0 | +1 | dB |
| Channel Balance | $E_{BL}$ | Vol=+26~-40dB | | -1 | 0 | +1 | dB |
| Mute Level | MUTE | HW or SW Mute | | - | -75 | - | dB |

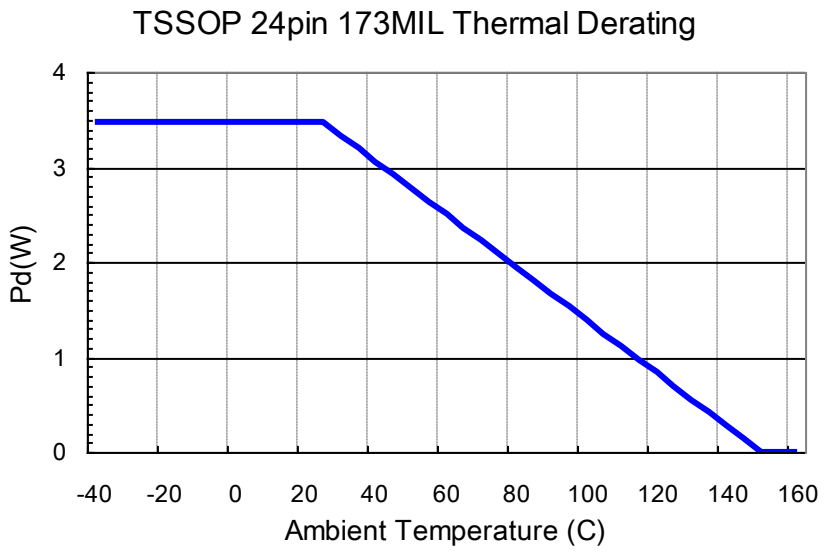
| Parameter | Symbol | Test Conditions | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| ***CLASS-AB AMPLIFIER*** | | | | | | | | |
| Total Harmonic Distortion | THD+N | Po=0.1W, RL=8Ω | | | - | 0.15 | - | % |
| | | Po=1W, RL=8Ω | | | - | 0.05 | - | |
| | | Po=0.1W, RL=4Ω | | | - | 0.15 | - | |
| | | Po=1W, RL=4Ω | | | - | 0.05 | - | |
| Output Power | Po | BTL | THD=1% | RL=8Ω | - | 1.3 | - | W |
| | | | | RL=4Ω | - | 2.1 | - | |
| | | | | RL=3Ω | - | 2.2 | - | |
| | | | THD=10% | RL=8Ω | - | 1.6 | - | |
| | | | | RL=4Ω | - | 2.6 | - | |
| | | | | RL=3Ω | - | 2.9 | - | |
| | | SE | THD=1% | RL=32Ω | - | 100 | - | mW |
| | | | THD=10% | RL=32Ω | - | 130 | - | |
| Load Resistance | RL | | | | 3 | 4 | - | Ω |
| Output DC Offset | Vos | BTL terminal | | | - | 5 | 10 | mV |
| | | From -40~+26dB | | | - | 0 | 2 | mV |
| Signal to Noise Ratio | SNR | PO=1.1W/8Ω, Gain=0dB | | | - | 95 | - | dB |
| Residual Noise | Vno | +26dB, BTL, A-weighted | | | - | 150 | - | μV |
| | | +20dB, SE, A-weighted | | | - | 75 | - | μV |
| | | +6dB, BTL, A-weighted | | | - | 30 | - | μV |
| | | 0dB, SE, A-weighted | | | - | 15 | - | μV |
| Channel Separation | CS | F=1KHz | | | - | 90 | - | dB |
| Supply Rejection Ratio | PSRR | F=200Hz, CB=1μF | | | - | 60 | - | dB |
| Thermal Protection | TSD | Output OFF | | | - | 150 | - | ℃ |
| | | Output ON | | | - | 90 | - | |
| ***CONTROL INTERFACE*** | | | | | | | | |
| Mute Active | MUTE | MUTE ON | | | 2 | - | - | V |
| | | MUTE OFF | | | - | - | 0.8 | |
| Pull Down Resistance | RDN | Mute pin | | | - | 300 | - | KΩ |
| Shutdown | SD | Shutdown OFF | | | 2 | - | - | V |
| | | Shutdown ON | | | - | - | 0.8 | |
| SE/BTL | SE/BTL | SE→BTL | | | 0.85 | 0.9 | - | VDD |
| | | BTL→SE | | | - | 0.5 | 0.6 | |
| $I^2C$ Bus Clock Rate | Fclk | VDD=3~5V | | | - | 100 | 500 | KHz |
| $I^2C$ Low Level | VIL | VDD=3~5V | | | - | - | 0.8 | V |
| $I^2C$ High Level | VIH | VDD=3~5V | | | 2 | - | - | V |
| $I^2C$ Input Current | IIN | VDD=3~5V | | | -5 | - | 5 | μA |
| SDA Pull Down Voltage | Vack | Rpull up=1KΩ, Ack active | | | - | 0.4 | - | V |

# PACKAGE THERMAL CHARACTERISTIC

## HTSSOP-24, 173MIL BODY WIDTH, WITH THERMAL PAD ON BOTTOM SIDE

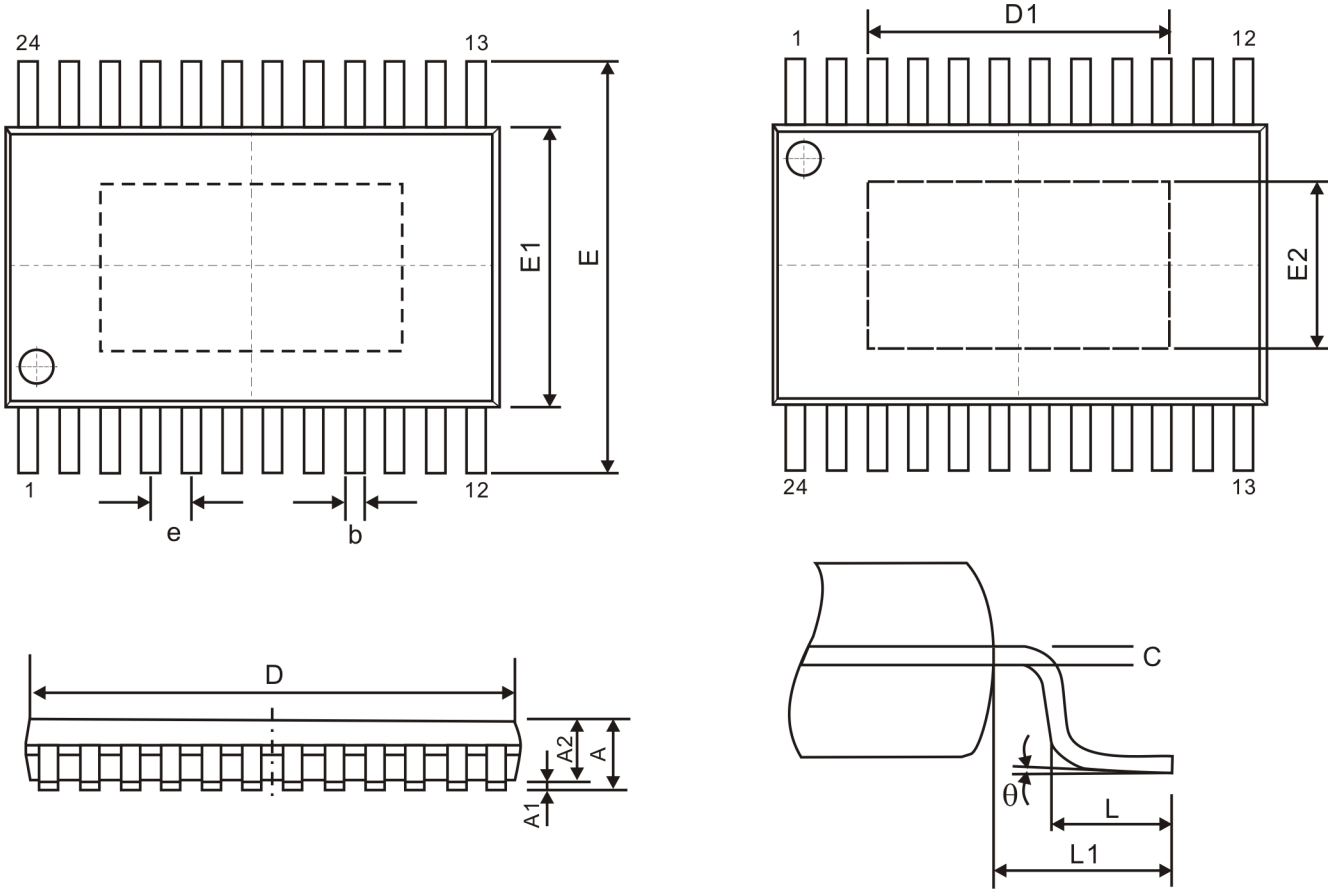
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance, Junction to Ambience (see note) | θja | Ta=25℃ | - | 36 | - | ℃/W |
| Power Dissipation Rating | Pdr | Ta≤25℃ | - | 3.4 | - | W |
| | | Ta=60℃ | - | 2.5 | - | |
| | | Ta≤85℃ | - | 1.8 | - | |

Note: The thermal resistance is measured on PTC evaluation board; the chip is mounted on a board with 2 layers, 1oz copper foil, the thermal pad must be soldered and board area greater than 2 $Inch^2$.



# PACKAGE INFORMATION

## *24 PINS, HTSSOP, 173MIL*




| Symbol | Min. | Nom. | Max. |
|---|---|---|---|
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| C | 0.09 | - | 0.20 |
| b | 0.19 | - | 0.30 |
| D | 7.70 | 7.80 | 7.90 |
| D1 | 2.70 | - | - |
| E | 6.30 | 6.40 | 6.50 |
| E1 | 4.30 | 4.40 | 4.50 |
| E2 | 1.50 | - | - |
| e | 0.65 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF. | | |
| θ | 0° | - | 8° |

Notes:

1. Refer to JEDEC MO-153.
2. All dimensions in millimeters.

## IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian, Taipei 23145, Taiwan
Tel: 886-2-66296288
Fax: 886-2-29174598
http://www.princeton.com.tw