FUJITSU

4-BIT MICROCOMPUTERS for DIGITAL TUNING SYSTEMS (CMOS)

MB88560 SERIES

April 1987
Edition 2.0

DESCRIPTION

The Fujitsu MB88560 series is an upgraded version of the MB88500 family and consists of two 4-bit microcomputers—the MB88561 with an LCD display controller/driver and the MB88562 with a VFD display driver. The architecture of each device (MB88561 and MB88562) is similar to counterpart products in the MB88500 series; however, to improve both flexibility and efficiency, an A/D converter, a phase locked loop (PLL), and on-chip display drivers are added. When high quality and low cost are primary design considerations, the MB88561 and/or the MB88562 is an excellent choice for digital tuning systems such as those used in automobile radios, stereo tuners, and other similar applications.

The MB88561 LCD device contains a 3K by 8-bit mask ROM (program memory) and a 192 by 4-bit static RAM (data memory) whereas, the MB88562 VFD device contains a 4K by 8-bit mask ROM and a 256 by 4-bit static RAM. Besides the on-chip memory, each device has 21 I/O lines, an 8-bit timer/counter, an A/D converter with 6-bit resolution, display drivers, and a phase locked loop (PLL) that is suitable for all broadcast and shortwave frequencies. Each device has independent AM (up to 32 MHz) and FM (up to 120 MHz) inputs.

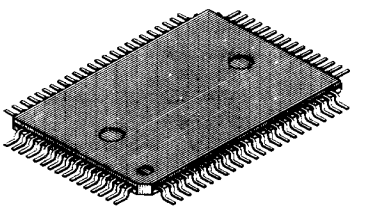
Controller/driver circuits of the MB88561 can directly drive 1/2 duty, 1/2 bias, 20-millisecond frame-cycle LCD devices; 52-segment LCD displays are available. VFD driver ports of the MB88562 are N-channel middle-voltage outputs with pull-down resistors; with a 12-volt power supply, these outputs can directly drive 39-segment VFD devices.

Mask options for the MB88560 series are shown in the following table. These options must be specified by the Customer when a device is ordered; data release forms for specifying the options are available at Fujitsu Sales Offices.

Both devices are fabricated in silicon-gate CMOS and are housed in an 80-pin plastic flat package. The MB88561 and MB88562 require a +5V power supply and operate over a temperature range of -40°C to +85°C.

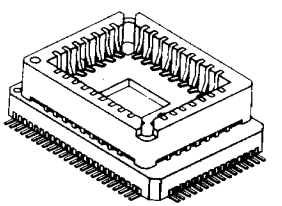
To minimize system cost and development time, Fujitsu provides a complete complement of hardware and software development tools— refer to "Table 1. Specification Summary and Development Tools."

MB88561-PF/MB88562-PF



80-PIN PLASTIC FLAT PACKAGE
(FPT-80P-M01)

MB88PG561-CF/MB88PG562-CF



80-PIN CERAMIC MODULE
(MQP-80C-P01)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

USER MASK OPTIONS

Function	Option	Remarks	Function	Option	Remarks
Output port type	Standard open-drain Standard pullup	Selected output port option must be the same for all P- and R-ports	Standby off reset	No Yes	
Standby	No Yes (software initiated)		Output port level during reset	High Low	R10 to R8 fixed high
Output port state during standby	Hold High-Z	Selected port-state option must be the same for all P-and R-ports	Pull-down resistor for segment output port	No Yes	MB88562 Only

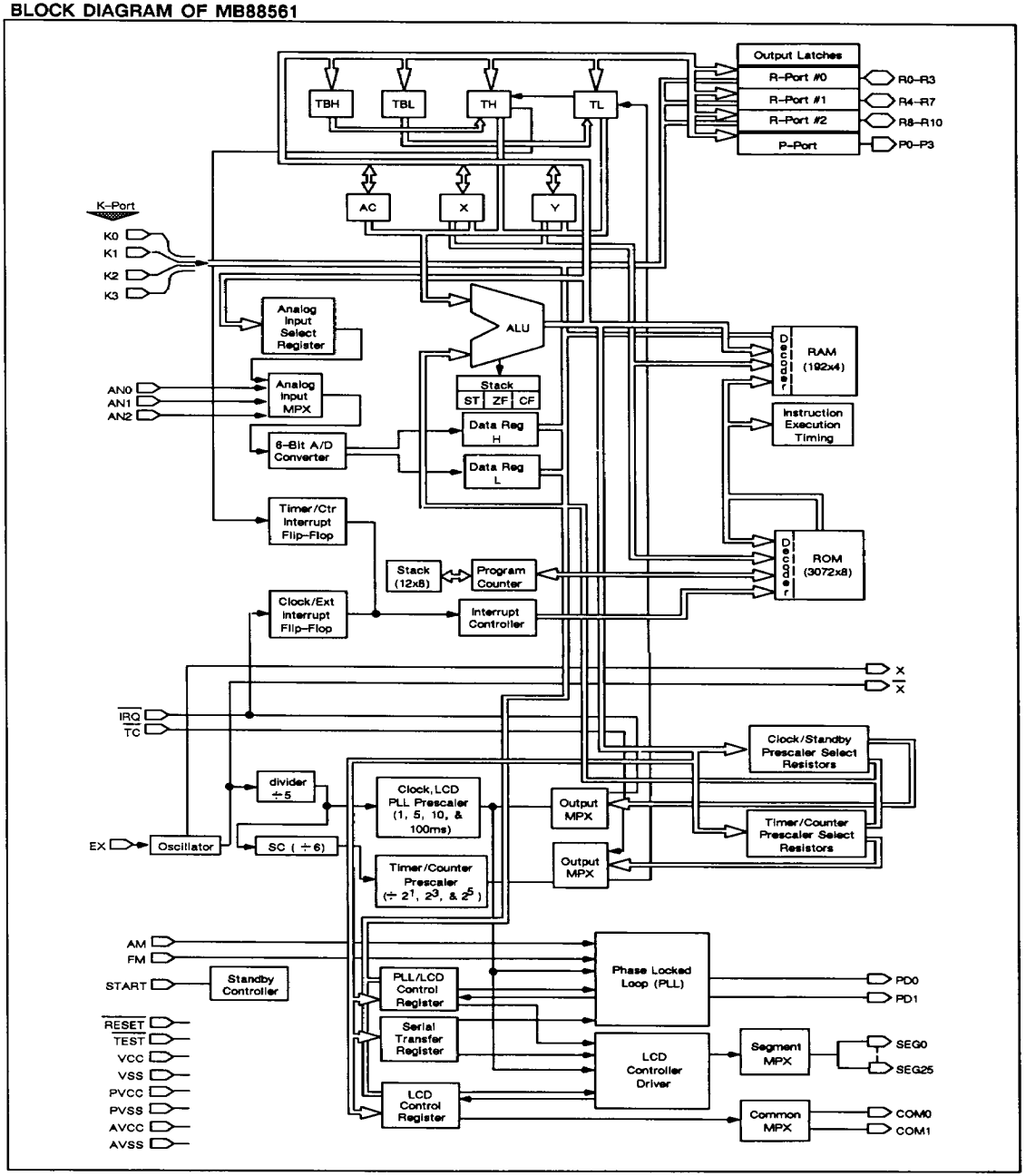
FEATURES

- Program Memory
  - MB88561: 3K x 8-bit mask ROM
  - MB88562: 4K x 8-bit mask ROM
- Data Memory
  - MB88561: 192 x 4-bit static RAM
  - MB88562: 256 x 4-bit static RAM
- 21 I/O Ports
  - P-port: 4-bit parallel output only
  - K-port: 4-bit parallel input only
  - R-port: Two 4-bit and one 3-bit parallel input/output or 11 individual input/output lines
  - C-port: External interrupt input; timer/counter input
- Two Selectable Output Port Circuits (P and R Ports—Mask Options):
  - Standard open drain
  - Standard pullup
- 8-Bit Programmable Timer/Counter with Auto-Load Function and Two Clock Modes:
  - Internal clock (timer)
  - External clock (counter)
- 6-Bit Programmable A/D Converter with 3 Multiplexed Analog Inputs and Sample/Hold Circuits (Successive Approximation Type Converter)
- On-Chip Phase Locked Loop (PLL) for Digital Tuning Systems:
  - 15-bit prescaler
  - 4.5 MHz reference frequency
  - Independent AM and FM input terminals
  - Two phase detector outputs
- Single Level Three Source Maskable Interrupt:
  - External
  - Clock
  - Timer/counter overflow
- Instruction Set (Upward compatible with MB88500 Series):
  - Number of instructions: 70 for MB88561; 71 for MB88562
  - Instruction byte length/cycle count: 1/1, 2/2, and 2/3
- Execution time: 6.67 µs (min) using 4.5 MHz clock
- Four Nesting Levels for Subroutine Calls
- Software Initiation of Low-Power Standby
- Selectable Output Port States During Standby (Mask Option):
  - Hold
  - High impedance
- Oscillator Programmable States During Standby:
  - Idle
  - Stop
- Other Mask Options:
  - Standby off reset
- On-Chip Power-On Reset
- On-Chip Clock Generator and 1/2 Clock Prescaler
- MB88561—On-Chip Liquid Crystal Display (LCD) Controller/Driver:
  - Direct drive for LCD.
  - Two common outputs and 26 segment outputs.
  - 13 x 4-bit display memory independent of data memory space.
  - Segment data table can be stored in program memory (mask ROM).
  - 1/2 duty and 1/2 bias (on-chip LCD bias circuits).
- MB88562—On-chip Vacuum Fluorescent Display (VFD) Driver:
  - Direct drive for 39-segment VFD (+12Vdc).
  - N-channel middle-voltage outputs with pull-down resistors.
- Low Power Dissipation:
  - MB88561 (Active Mode)—27.5 mA (max) with following conditions:
    f_C = 4.5 MHz
    VCC = AVCC = PVCC = 5.5V
  - MB88561 (Standby Mode)—30 µA (max) with
    f_C = 0 MHz
    VCC = AVCC = PVCC = 6.0V
  - MB88562 (Active Mode)— 42.5 mA (max) with following conditions:
    f_C = 4.5 MHz
    VCC = PVCC = 5.5V; SEGVCC = 12.5V
  - MB88562 (Standby Mode)—20 µA (max) with
    f_C = 0 MHz
    VCC = PVCC = 6.0V
- Powerful Development Support (refer to Table 1)
- Wide Range of Operating Temperatures: T_A = -40°C to +85°C.
- 80-Pin Plastic Flat Package: FPT-80P-M01

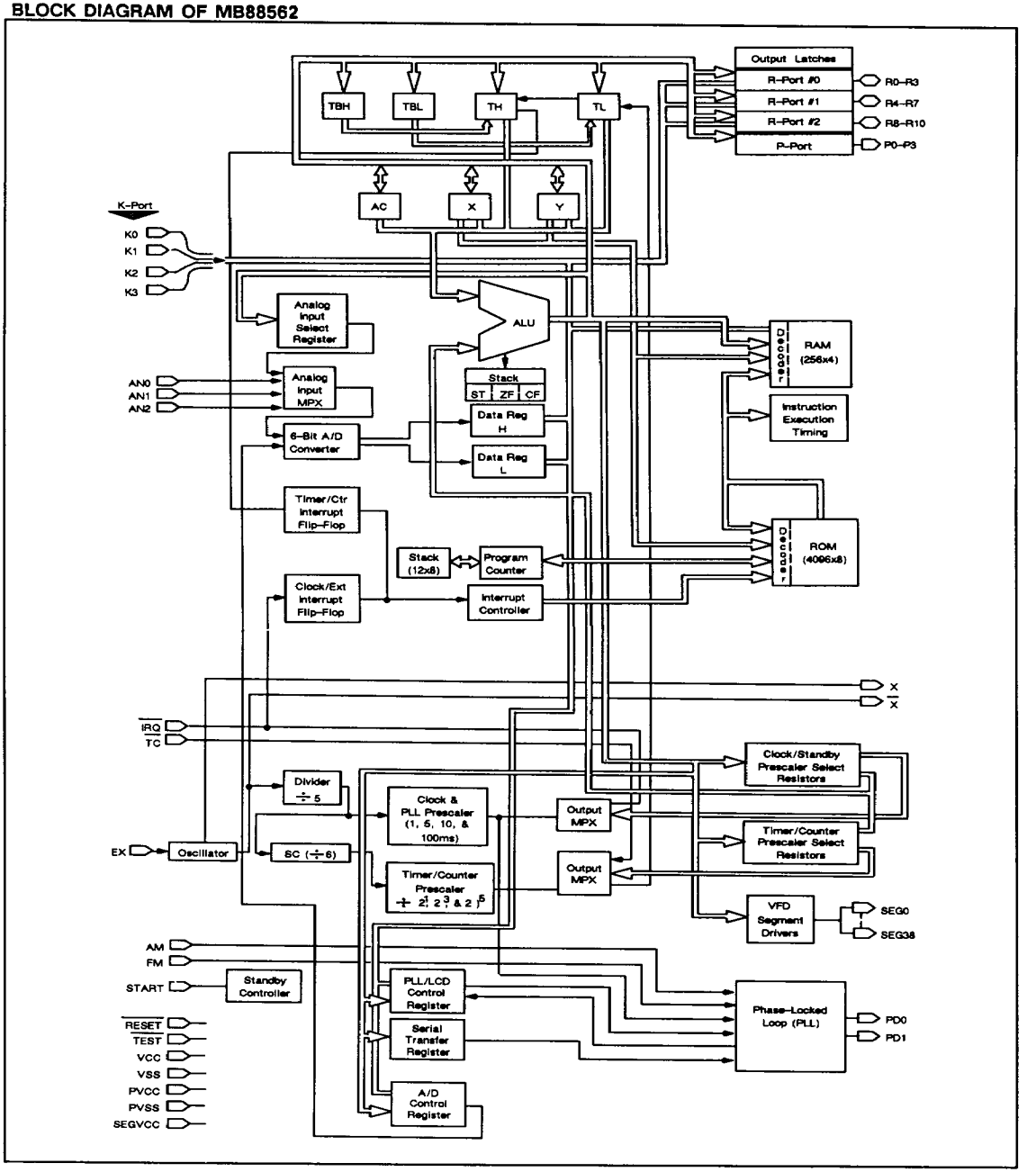
Table 1. Specification Summary and List of Development Tools

	MB88561-PF	MB88562-PF
ROM size	3K x 8 bits (On-chip mask ROM)	4K x 8 bits (On-chip mask ROM)
RAM size (Directly addressed locations)	192 x 4 bits (Addresses 0-7)	256 x 4 bits (Addresses 0-7)
I/O port:	Total 21 lines	Total 21 lines
Input-only port	4	4
Output-only port	4	4
I/O port	11	11
Control port	2	2
Output port type	Standard pull-up Standard open-drain (Mask option)	Standard pull-up Standard open-drain (Mask option)
Stack depth (Nesting level)	4 levels	4 levels
Timer/Counter: Buffer size Clock source	Yes (Auto Load function) 8 bits Internal/External	Yes (Auto Load function) 8 bits Internal/External
Serial I/O	No	No
Clock generator: Oscillator type Clock frequency	Yes Crystal/External 4.5MHz	Yes Crystal/External 4.5MHz
Interrupt function: Nesting level Interrupt sources	Yes Single level 3 sources	Yes Single level 3 sources
Standby function: Initiation method Oscillator state during standby Output state during standby Standby off reset function	Yes/No (Mask option) Software Idle or stop (Software selectable) Hold or High- Z (Mask option) Yes/No (Mask option)	Yes/No (Mask option) Software Idle or stop (Software selectable) Hold or High- Z (Mask option) Yes/No (Mask option)
Watch dog timer function	No (Fixed)	No (Fixed)
Number of instructions	70	71
Instruction byte length/ cycle count	1/1, 2/2, or 2/3	1/1, 2/2, or 2/3
Instruction execution time	6.67 µs (min) at 4.5 MHz (With prescaler)	6.67 µs (min) at 4.5 MHz (With prescaler)
Power supplies: Active Standby	 4.5V to 5.5V (VCC=PVCC=AVCC) 3.5V to 6.0V (VCC=PVCC=AVCC)	4.5V to 5.5V (VCC=AVCC); 11.5V to 12.5V (SEGVCC) 3.5V to 6.0V (VCC=AVCC)
Operating temperature range	-40°C to +85° C	-40°C to +85° C
Process	CMOS	CMOS
Package	80-pin FPT	80-pin FPT
Development tools: Hardware	MB2115-01 : CRT unit (MB88561 and MB88562) MB2115-02 : Monitor board with keyboard (MB88561 and MB88562) MB2115-04 : EPROM writer/RS232C interface unit (MB88561 and MB88562 MB2115-40 : DUE board (for MB88561) MB2115-41 : DUE board (for MB88562)	
Software	MB88PG561-CF : Piggyback evaluation device (for MB88561) MB88PG562-CF : Piggyback evaluation device (for MB88562) SM05215-A010 : Intellec series II/III MDS cross-assembler SM07415-A012 : CP/M-86 cross-assembler SM07615-AXXX : PC-DOS cross-assembler SM07415-G022 : CP/M-86 host emulator SM07615-GXXX : PC-DOS host emulator	

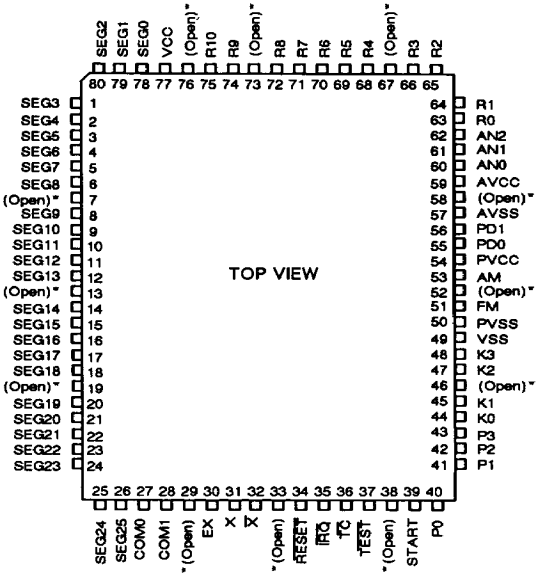
BLOCK DIAGRAM OF MB88561



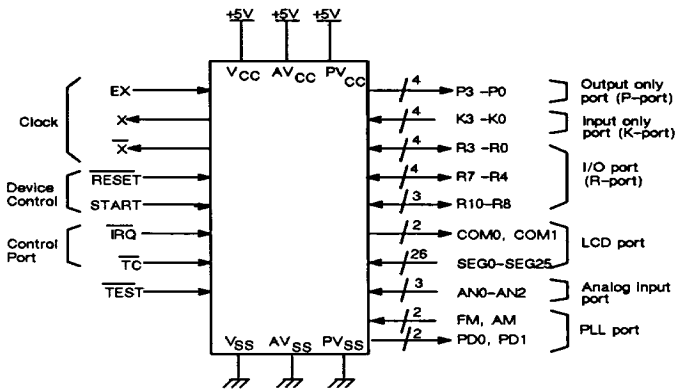
BLOCK DIAGRAM OF MB88562



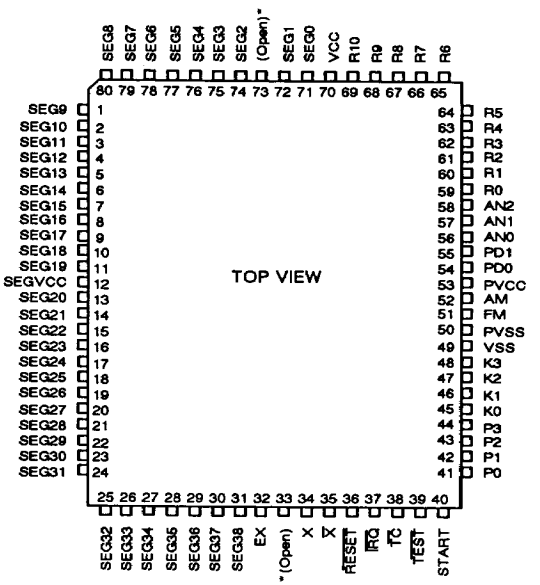
PIN ASSIGNMENTS & INTERFACE CONNECTIONS FOR MB88561



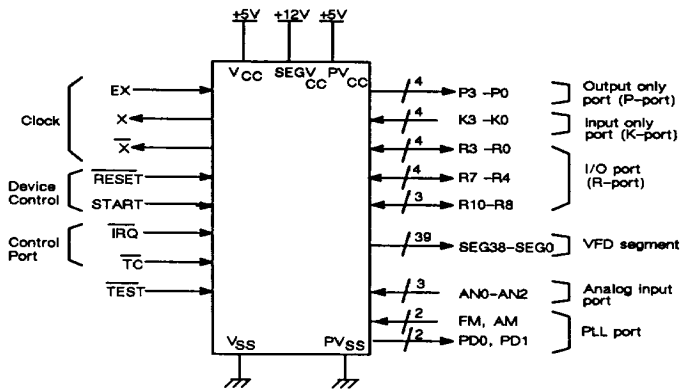
*These pins are not connected.



PIN ASSIGNMENTS & INTERFACE CONNECTIONS FOR MB88562



*These pins are not connected.



PIN DESCRIPTIONS

Pin No.		Designator	Function
MB88561	MB88562		
77	70	VCC	+5V DC power supply.
49	49	VSS	Ground.
30	32	EX	Input to on-chip oscillator. A 4.5 MHz crystal is externally connected between the EX and X pins.
31	34	X	Output of on-chip oscillator; input for the internal clock generator.
32	35	$\overline{X}$	Provides an inverted clock output for external sync functions.
34	36	$\overline{RESET}$	An external reset input and a power-on reset output. When set to a LOW logic level, halts operation of the MCU and initializes the device. When the $\overline{RESET}$ pin returns to a HIGH logic level, program execution restarts at address 0. When the oscillator stabilizes after power-on, the $\overline{RESET}$ pulse must be LOW for at least two instruction cycles to properly initialize the device. To implement an external reset, connect a capacitor between the $\overline{RESET}$ pin (internal pull-up resistor) and ground (VSS pin); the time constant should be greater than the time interval of 12 clock periods. When the device is powered up, the on-chip reset control circuit outputs a Low level on this pin. Except for the reset mode, the output is High during normal operation. The rise of VCC (50µs to 50ms of rise time) causes a Low output from the $\overline{RESET}$ pin; it automatically returns to a High state approximately 80-milliseconds after the on-chip oscillator starts. The $\overline{RESET}$ pin is a hysteresis input with an internal 300k-ohm pullup resistor.
39	40	START	Release input for the standby control/status registers; these registers monitor and control the on-chip standby control circuits. During the standby mode, a HIGH level on the START pin sets the standby release flag (STF) in the standby status register, resets the standby enable flag (STBE) in the standby control register and triggers the sequence that returns the MCU to an active mode. Before the START pulse is applied, VCC must return to the normal operating range (+5V ± 10%) when a backup battery is used. Also, the START pin must be LOW before initiating the standby mode. The logical state of the START pin can be sensed by executing an IN instruction (Y=8) to read the standby status register. The logic level is indicated by the standby release input flag (STIF). The START pin is a hysteresis input with an internal 300k-ohm pullup resistor.
35	37	$\overline{IRQ}$	Maskable external interrupt input to the on-chip interrupt control circuit. The falling edge of $\overline{IRQ}$ sets the external interrupt request flag ($\overline{IRF}$) in the interrupt flag register regardless of whether the external interrupt is enabled or disabled. If the external interrupt is enabled in advance by an EN instruction, the interrupt is immediately serviced; if not enabled, the IRF flag is internally held as an interrupt source. The logic level of the $\overline{IRQ}$ pin can be tested with a TSTI instruction; when $\overline{IRQ}$ is LOW, the interrupt flag (IF) is HIGH. For all other conditions, IF is LOW. The $\overline{IRQ}$ pin is a hysteresis input with an internal 300k-ohm pullup resistor.
36	38	$\overline{TC}$	Clock-count input pulses to the on-chip 8-bit timer/counter. The falling edge of $\overline{TC}$ increments the timer/counter by one count under the following conditions: • When external count clock (counter) mode is selected by EN instruction. • When timer/counter prescaler select register is programmed to enable the $\overline{TC}$ input using OUT instruction (Y=B). OUT instruction (Y=B). The $\overline{TC}$ pin is inactive as a clock-count input when the external clock-count mode is disabled by RESET or by a DIS instruction, or the $\overline{TC}$ input is not selected by the timer/counter prescaler select register. The logic level of the $\overline{TC}$ pin is always indicated by the timer/counter input flag (TCIF) in the timer/counter prescaler select register. The logic level of the $\overline{TC}$ pin can be tested by using an IN instruction (Y=B) to read the prescaler select register; when $\overline{TC}$ is LOW, the TCIF flag is HIGH. For all other conditions, TCIF is LOW. The $\overline{TC}$ pin is a hysteresis input with an internal 300k-ohm pull-up resistor.

PIN DESCRIPTIONS (Cont'd)

Pin No.		Designator	Function
MB88561	MB88562		
48–47, 45–44	48–47, 46–45	K3–K0	K-port. A 4-bit parallel non-latched input-only port; K0 is LSB. K-port data is input to accumulator via an INK instruction. All K-port pins have internal pullup resistors.
43–40	44–41	P3–P0	P-port. A 4-bit parallel latched output-only port; P0 is LSB. Data from the accumulator is output to the P-port via an OUTP instruction. Refer to DESCRIPTION for available masking options.
66–63 71–68 75–74, 72	62–59 66–63 69–67	R3–R0 R7–R4 R10–R8	The R-port serves as two 4-bit and one 3-bit parallel non-latched inputs/latched outputs or 11 individual non-latched input/latched output lines. The selected service depends on the sequence of instructions. Using the parallel I/O structure, the two 4-bit ports are designated R-port #0 (R3–R0) and R-port #1 (R7–R4); the 3-bit port is designated R-port #2 (R10–R8). All three ports are indirectly addressable by port number via the Y-register. Four-bit (or three-bit) data from the accumulator is output to the addressed R-port via an OUT instruction; four-bit (or three-bit) data from one port is input to the accumulator via an IN instruction. Before executing an IN instruction, the addressed port must be set to a High (input) mode) logic level. When the R-port lines are used individually, each line (R10–R0) can be indirectly addressed by bit number via the Y-register Each addressed bit line can be set or reset by a SETR/RSTR instruction; the lines of R-port #0 (R3–R0) can be directly set or reset by a SETD/RSTD instruction. Each addressed line is individually testable by a TSTR instruction; each line of R-port #2 can be directly tested with a TSTD instruction. Before executing a TSTD or TSTR instruction, the addressed bit line must be set to a High (input mode) logic level. Refer to description for available mask options.
37	39	$\overline{\text{TEST}}$	Used to activate the test mode for the purpose of shipping tests at Fujitsu. This pin is normally set to a High logic level with an internal pullup.

Pin No.		Designator	Function
MB88561	MB88562		
7, 13, 19, 29, 33, 38, 46, 52, 58, 67, 73, 76	33, 73	Open	No connection to these pins.
59	--	AVCC	+5V DC power supply voltage for A/D converter.
57	--	AVSS	Ground pin for A/D converter.
62–60	58–56	AN2–AN0	A/D converter inputs. One of three analog input ports is selected via the analog input select register (Y = D). The A/D converter is activated by writing a "1" to bit #0 of the A/D control register (Y = 9). When conversion is complete, the high-order bits are placed in the A/D data register (Y=F) and the low-order two bits are put into the A/D data register (Y=E).
54	53	PVCC	+5VDC power supply voltage for PLL.
50	50	PVSS	Ground pin for PLL.
51	51	FM	Local oscillator inputs. The PLL consists of a reference clock generator prescaler, a local oscillator clock-programmable prescaler and a comparator. The reference clock frequency can be selected from any-one of the following: 25 kHz, 12.5 kHz, 10 kHz, 9 kHz, 5kHz, or 1.0 kHz. Local oscillator input for FM. The local oscillator programmable prescaler has a 15-bit pulse swallow divider. The FM local frequency is input to the FM terminal.
53	52	AM	Local oscillator input for AM. A 15-bit pulse swallow divider and also a direct divider are provided for the local oscillator programmable prescaler; the prescaler can be selected by software The AM local frequency is input to the AM terminal.
55–56	54–55	PD0, PD1	Phase comparison error outputs. Signals from the local oscillator input and the reference clock are compared; the error signal is output on PD0/PD1.
27,28	--	COM0, COM1	Common outputs for Liquid Crystal Display (LCD). Two one-half duty cycle, one-half bias LCD drivers are used for common outputs.

2

PIN DESCRIPTIONS (Cont'd)

Pin No.		Designator	Function
MB88561	MB88562		
26–20, 18–14, 12–8, 6–1, 80–78	--	SEG25–SEG0	Segment outputs for LCD. Twenty six one-half duty cycle, one-half bias LCD drivers are used for segment outputs. In addition to internal RAM, an on-chip segment data memory of 13 x 4 bits is available to store the display data.
--	12	SEGVCC	12V DC power supply for VFD driver segment output.
--	75, 74, 72, 71	SEG 3-0	Segment port. These lines serve as nine 4-bit and one 3-bit parallel latched output-only ports for VFD segments.
	79–76	SEG 7-4	
	3–1, 80	SEG 11-8	
	7–4	SEG 15-12	

Pin No.		Designator	Function
MB88561	MB88562		
	11–8	SEG 19–16	The 4-bit ports are consecutively designated SEG port #0 (SEG 3–0) through SEG port #8 (SEG 35–32); the 3-bit port is designated as SEG port #9 (SEG 39–36). The ports are indirectly addressable by port number via the Y-register. Data from the accumulator is output to an addressed port (SEG port #0 through SEG port #9) by an OUTX instruction. The SEG ports are middle-voltage outputs with pull-down resistors and are driven Low by a RESET pulse.
	16–13	SEG 23–20	
	20–17	SEG 27–24	
	24–21	SEG 31–28	
	28–25	SEG 35–32	
	31–29	SEG 39–36	

OPERATIONAL GUIDELINES

To achieve optimum performance and to minimize the chances of device failure, the MB88561 and/or the MB88562 should be used within the operating boundaries described in subsequent paragraphs.

Device Latchup

If latchup occurs, the supply current may increase to the point of thermal destruction. To prevent latchup, the operational limits and procedures specified below should be followed.

- Never apply a voltage higher than VCC or lower than VSS to any input or output pin.
- Voltages exceeding Absolute Maximum Ratings should not be applied between VCC and VSS pins—Refer to ELECTRICAL CHARACTERISTICS.
- Do not power-up MCU power supply (VCC) until power has been applied and is stabilized for the analog power supply (AVCC), PLL power supply (PVCC), and the VFD power supply (SEGVCC).

Supply Voltages

Abrupt changes in the operating supply voltages can cause device malfunction; therefore, well-regulated power supplies should be used. The ripple and rate-change values should not exceed the following:

- The peak-to-peak VCC ripple at commercial frequencies of 50–60 Hz should be less than 10% of the typical value of VCC.
- The transient change rate of VCC should be less than 0.1V/ms.

Unused Input Pins

Unused input pins should be pulled up-or-down with external resistors; However, the X pin should be open when an external clock is used.

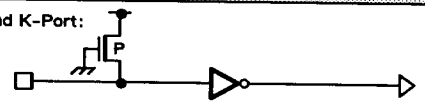
$\overline{\text{TEST}}$ Pin

This input pin is used to activate the test mode for shipping test purposes at Fujitsu. When the $\overline{\text{TEST}}$ pin is forced to a low logic level while the $\overline{\text{RESET}}$ pin is low, the device enters the test mode. To prevent undesired activation of the test mode during normal operation, an external pull-up resistor is recommended in addition to the internal 10k-ohm pullup.

INPUT/OUTPUT CIRCUITS

Input Only Port & Control Port

IRQ, $\overline{TC}$, and K-Port:

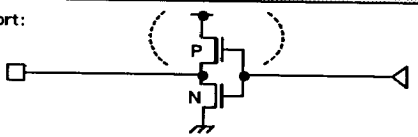


Description: Input pullup resistor (P-channel transistor). Typically 300K-ohms at VCC=5V. Hysteresis inverter for IRQ and $\overline{TC}$.

AM and FM:

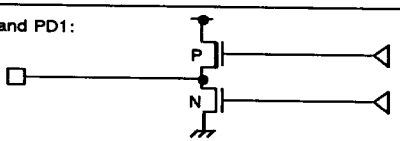
Output Only Port

P-Port:



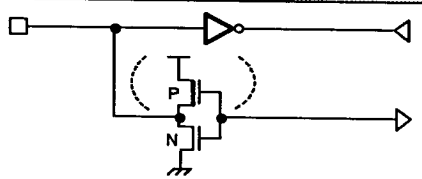
Description: Output options are standard pullup and standard open-drain. For standard pullup, the pullup resistor is a P-channel transistor that typically represents about 10K-ohms at VCC=5V. In an open-drain configuration, the pullup resistor is omitted.

PD0 and PD1:



Input/Output Port

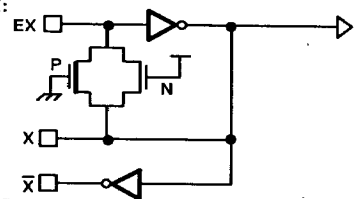
R-Port:



Description: Output options are standard pullup and standard open-drain. For standard pullup, the pullup resistor is a P-channel transistor that typically represents about 10K-ohms at VCC=5V. In an open-drain configuration, the pullup resistor is omitted.

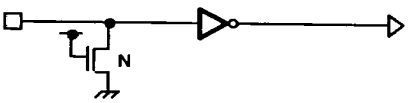
Crystal/Ceramic Oscillator

EX, X, and $\overline{X}$:



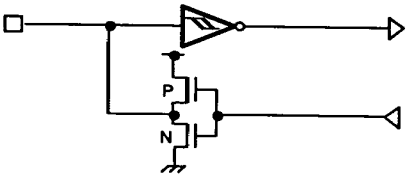
Description: Feedback resistor ≅ 2 Megohms.

START Circuit



Description: The pull-down resistor is an N-channel transistor that typically represents about 300K-ohms at VCC=5V. An hysteresis-type inverter is used.

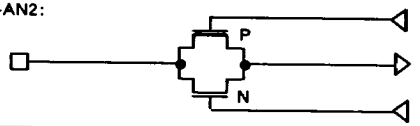
RESET Circuit



Description: The pullup resistor is a P-channel transistor that typically represents about 300K-ohms at VCC=5V. A hysteresis type inverter is used.

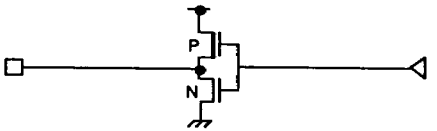
Analog Port

AN0–AN2:



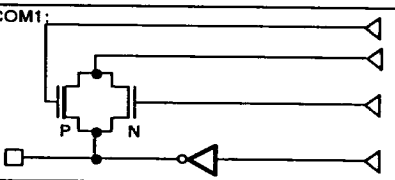
LCD Controller/Driver Port for MB88561

SEG0–SEG25:



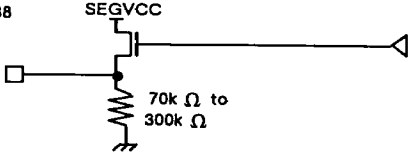
Description: The pullup resistor is a P-channel transistor that typically represents about 10K-ohms at VCC=5V.

COM0 and COM1:



VFD Driver Port for MB88562

SEG0–SEG38 SEGVCC



2

INSTRUCTION SET

The instruction set for the MB88560 microcomputer series consists of 70 instructions for the MB88561 and 71 instructions for the MB88562. Of the total, 84% are single-byte/single-cycle instructions. 15% are two-byte/single cycle instructions, 15% are two-byte/two-cycle instructions and 1% are two-byte/three-cycle instructions. The instruction set for the MB88560 series is upward compatible with that of the MB88500 series and, as shown in Table 3, is divided into ten functional groups. Symbols and abbreviations that are commonly used in the instruction set are shown Table 2. Table 3 provides a summary of operational data and all instruction codes are summarized in Table 4.

Table 2. Symbols and Abbreviations Used In Instruction Set

Symbols	Meaning
←	Is transferred to
↚	Is exchanged with
+	Arithmetic plus
−	Arithmetic minus
⊕	Logical EXCLUSIVE OR
∩	Logical OR
∪	Logical AND
$\overline{\quad}$ (overline)	Negation
( )	Contents of parenthesis
↑	Set to "1" always
↓	Set to "0" always
↕	Affected (set or reset) by operation results
↓C	Set to "0" due to carry (not carry flag)
↓IF	Set to "0" due to interrupt flag
↓CF	Set to "0" due to carry flag
↓VF	Set to "0" due to timer/counter overflow flag
↓Z	Set to "0" due to zero (not zero flag)
↓ZF	Set to "0" due to zero flag
·	Not affected

Abbreviation	Meaning
AC	Accumulator
addr	Jump address
bp	Bit pointer (that is part of the instruction code)
C	Carry
CF	Carry flag
d	Direct line number (that is part of the instruction code)
IF	Interrupt flag
imm	Immediate data
$\overline{IRQ}$	Interrupt request
K	K-Port (K3 to K0)
LSB	Least significant bit
M(X,Y)	Data memory (RAM) location indirectly addressed by data pointer (X- and Y- registers)
M(0,D)	Data memory (RAM) location directly addressed by "D" bits in the instruction code in page #0 (X=0)
MSB	Most significant bit
P	P-Port (P3 to P0)
R	R-Port (#0: R3-R0, #1: R7-R4, #2: R10-R8)
(R)Y; Y=n	[1] R-Port #n specified by Y-register (Y=0 to 3) [2] R-Port bit n specified by Y-register (Y=0 to 10)
(R)d; d=n	R-Port bit n specified by "d" bits in the instruction code
SEG	Segment port (#0: SEG3-SEG0, ...#7: SEG39-SEG36) :MB88562
ST	Status flag
TH	Timer/counter high byte
TL	Timer/counter low byte
VF	Timer/counter overflow flag
X	X-register (that indicates page # in data memory RAM)
Xn	The n-th bit X-register
Y	Y-register
Z	Zero
ZF	Zero flag

Table 3. Instruction Set Summary

Mnemonic + Operand	Execution Code (In Hex)	Byte/ Cycle	Flag/Status ZF	CF	ST	Operation
Register-to-Register Transfer						
TATH	05	1/1	·	·	·	TH←(AC)
TATL	06	1/1	·	·	·	TL←(AC)
TAY	04	1/1	·	·	·	Y←(AC)
TTHA	15	1/1	‡	·	·	AC←(TH)
TTLA	16	1/1	‡	·	·	AC←(TL)
TYA	14	1/1	‡	·	·	AC←(Y)
XX	1B	1/1	‡[1]	·	·	(AC)↔(X)
Register-to-Memory Transfer						
L	0D	1/1	‡	·	·	AC←{M(X,Y)}
ST	1D	1/1	·	·	·	M (X,Y) ←(AC)
STDC	1A	1/1	·	·	↓C	M(X,Y) ←(AC), Y←(Y)-1
STIC	0A	1/1	·	·	↓C	M(X,Y) ←(AC), Y←(Y)+1
X	0B	1/1	‡[1]	·	·	(AC)↔{M(X, Y)}
XD D	50-53	1/1	‡[1]	·	·	(AC)↔{M(0, D)} ; D = 0 to 3 (X = 0, Y = D)
XYD D	54-57	1/1	‡[2]	·	·	(Y)↔{M(0, D)} ; D = 4 to 7 (X = 0, Y = D)
Constant Transfer						
CLA	90	1/1	↑	·	·	AC← 0 (Included in LI instruction)
LI imm	90-9F	1/1	‡	·	·	AC←imm; imm=0 to 15
LXI imm	58-5F	1/1	‡	·	·	X3←0, X2 to X0←imm; imm=0 to 7
LXID imm	3D90-3D9F	2/2	‡	·	·	X←imm; imm = 0 to 15
LRXA imm	3D20-3D3F	2/3	·	·	·	X←{ROM (imm X Y)} d, d = 7-4 AC←{ROM(imm X Y)} d, d = 3-0 imm = 0 to 15[4]
LYI imm	80-8F	1/1	‡	·	·	Y←imm; imm = 0 to 15
Arithmetic & Logical Operations						
ADC	0E	1/1	‡	‡	↓C	AC←(AC) +{ M(X,Y)} + (CF)
AI imm	3D80-3D8F	2/2	‡	‡	↓C	AC←(AC) + imm; imm=0 to 15
AND	0F	1/1	‡	·	↓Z	AC←(AC)∩{ M(X, Y)}
C	2E	1/1	‡	‡	↓Z	{ M(X, Y) }- (AC)
CI imm	B0-BF	1/1	‡	‡	↓Z	imm- (AC); imm = 0 to 15
CYI imm	A0-AF	1/1	·	·	↓Z	imm- (Y); imm = 0 to 15
DAA	10	1/1	‡	·	↓C	AC← (AC) +6 if (AC)>9 or (CF) = 1
DAS	11	1/1	‡	·	↓C	AC←(AC) +10 if (AC) >9 or (CF) = 1
DCA	3D8F	2/2	‡	‡	↓C	AC←(AC) + 15 (Included in AI instruction)
DCM	19	1/1	‡	·	↓C	M(X, Y)←{M(X, Y) } -1
DCY	18	1/1	·	·	↓C	Y←(Y)-1
EOR	2F	1/1	‡	·	↓Z	AC←{M(X, Y)}⊕ (AC)
ICA	3D81	2/2	‡	‡	↓C	AC←(AC) +1 (Included in AI instruction)
ICM	09	1/1	‡	·	↓C	M(X,Y)←{M(X,Y) }+1
ICX	3DAC	2/2	·	·	↓C	X←(X) +1
ICY	08	1/1	‡	·	↓C	Y←(Y) +1
NEG	2D	1/1	·	·	↓Z	AC←($\overline{AC}$) + 1

Table 3. Instruction Set Summary (Cont'd)

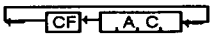
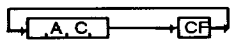
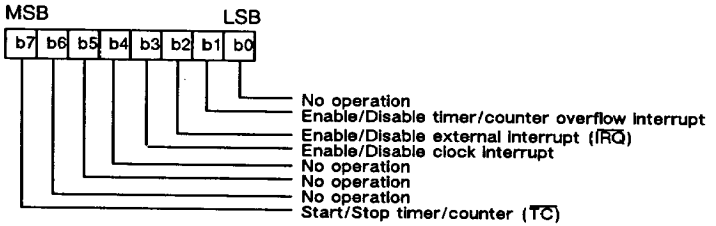
Mnemonic + Operand	Execution Code (In Hex)	Byte/ Cycle	Flag/Status ZF	CF	ST	Operation
Arithmetic & Logical Operations (Cont'd)						
OR	1F	1/1	↕	·	↓Z	AC←{M(X, Y)}∪ (AC)
ROL	0C	1/1	↕	↕	↓C	
ROR	1C	1/1	↕	↕	↓C	
SBC	1E	1/1	↕	↕	↓C	AC←{M(X, Y)} - (AC)-(CF)
Bit Manipulation						
RBIT bp	34-37	1/1	·	·	·	{M(X, Y)} bp← 0; bp = 0 to 3
SBIT bp	30-33	1/1	·	·	·	{M(X, Y)} bp← 1;bp = 0 to 3
RBA bp	3DA4-3DA7	2/2	·	·	·	(AC) bp← 0 ; bp = 0 to 3
SBA bp	3DA0-3DA3	2/2	·	·	·	(AC)bp← 1 ; bp = 0 to 3
TBA bp	4C-4F	1/1	·	·	↓Z	(AC)bp-1 ; bp = 0 to 3
TBIT bp	38-3B	1/1	·	·	↓Z	{M(X, Y)}bp-1; bp = 0 to 3
Control						
EN Imm	3E00-3EFF	2/2 [3]	·	·	·	Enable the internal resources by the operand byte (2nd byte) [3]
DIS Imm	3F00-3FFF	2/2 [3]	·	·	·	Disable the internal resources by the operand byte (2nd byte) [3]
RST	3DAD	2/2	·	·	·	System Initialization
Input/Output						
IN	13	1/1	↕	·	·	AC←(R)Y ; Y=0 to 3 (Port #)
INK	12	1/1	↕	·	·	AC←(REG)Y; Y=5, 6, 8, 9, B, C, E, F AC←(K)
OUT	03	1/1	·	·	·	(R)Y←(AC); Y=0 to 3 (Port #) (REG)Y←(R); Y=5, 6, 7, 8, 9, B, D
OUTP	02	1/1	·	·	·	P← (AC)
OUTX	3DAB	2/2	·	·	·	(SEG) Y← AC; Y=0 to 9 (MB88562 only)
RSTD d	44-47	1/1	·	·	·	(R)d←0; d=0 to 3 (Bit # of Port #0)
RSTR	22	1/1	·	·	·	(R)Y←0; Y=0 to 10 (Bit #)
SETD d	40-43	1/1	·	·	·	(R)d←1; d=0 to 3 (Bit # of Port #0)
SETR	20	1/1	·	·	·	(R)Y←1; Y=0 to 10 (Bit #)
TSTD d	48-4B	1/1	·	·	↓Z	(R)d-1; d=8 to 10 (Bit #)
TSTR	24	1/1	·	·	↓Z	(R)Y-1; Y=0 to 10 (Bit #)
Branch						
CALL addr	6000-6FFF	2/2	·	·	·	If ST=1, Subroutine Call for addr; addr=0 to 4095 [4] ST=0, No Subroutine Call
JMP addr	C0-FF	1/1	·	·	·	If ST=1, Branch to addr, addr=0 to 63; ST=0, No Branch
JPXY addr	3D00-3D1F	2/2	·	·	·	Branch always to addr on page #n;
JPL addr	7000-7FFF	2/2	·	·	·	If ST=1, Branch to addr, addr=0 to 4095 [4]; ST=0, No Branch
RTI	3C	1/1	·	·	·	Return From Interrupt Routine
RTS	2C	1/1	·	·	·	Return From Subroutine

Table 3. Instruction Set Summary (Cont'd)

Mnemonic + Operand	Execution Code (In Hex)	Byte/ Cycle	Flag/Status ZF	CF	ST	Operation
Flag Manipulation						
RSTC	23	1/1	·	↓	·	CF← 0
SETC	21	1/1	·	↑	·	CF← 1
TSTC	28	1/1	·	·	↓CF	(CF) -1
TSTI	25	1/1	·	·	↓IF	(IF)-1, (If $\overline{IRQ}$=L, IF=1)
TSTV	26	1/1	·	·	↓VF	(VF)-1, VF←0
TSTZ	29	1/1	·	·	↓ZF	(ZF)-1
Other						
NOP	00	1/1	·	·	·	No Operation

Notes:

1. ZF is set or reset depending upon contents of accumulator after instruction execution.
2. ZF is set or reset depending upon contents of Y-register after instruction execution.
3. Each bit of the second-byte operand functions as follows:



4. MB88561: Maximum program address is 3071, so the following instruction operands are restricted.

Mnemonic + Operand	Execution Code (In Hex)	Byte/ Cycle	Flag/Status ZF	CF	ST	Operation
CALL addr	6000-6BFF	2/2	·	·	·	If ST=1, Subroutine Call for addr; addr=0 to 3071 ST=0, No Subroutine call

JPXY addr	3D00-3D1B	2/2	·	·	·	Branch always to addr on page #n
						addr=0 to 3071

JPL addr	7000-7BFF	2/2	·	·	·	If ST=1, Branch to addr; addr=0 to 3071 ST=1, No Branch
LRXA imm	3D20-3D2B	2/2	·	·	·	X← { ROM([imm] [X] [Y])} d, d=7-4 AC← { ROM([imm] [X] [Y])} d, d=3-0 imm=0 to 15

Table 4. Instruction Codes Summary

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	NOT USED	OUTP	OUT	TAY	TATH	TATL	NOT USED	ICY	ICM	STIC	X	ROL	L	ADC	AND
1	DAA	DAS	INK	IN	TYA	TTHA	TTLA	NOT USED	DCY	DCM	STDC	XX	ROR	ST	SBC	OR
2	SETR	SETC	RSTR	RSTC	TSTR	TSTI	TSTV	NOT USED	TSTC	TSTZ	NOT USED	NOT USED	RTS	NEG	C	EOR
3	SBIT				RBIT				TBIT				RTI	EXT[1]	EN	DIS
4	SETD				RSTD				TSTD				TBA			
5	XD				XYD				LXI							
6	CALL												Note 2			
7	JPL												Note 2			
8	LYI															
9	(CLA)	LI														
A	CYI															
B	CI															
C	JMP															
D																
E																
F																

Extended Instruction

3DH \ 3DL	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JPXY addr															
1													Note 2			
2	LRXA imm												Note 2			
3	Not used															
4																
5																
6	Not used															
7																
8		(ICA)	AI imm													(DCA)
9	LXI imm															
A	SBA bp				RBA bp				Not Used			OUTX[2]	ICX	RST		
B	Not used															
C	Not used															
D																
E	Not used															
F																

Legend:
- 1-byte/1-cycle instruction
- 2-bytes/2-cycles instruction

Notes:
1. Refer to extended instruction below.
2. MB88562 only.

ELECTRICAL CHARACTERISTICS MB88561

Absolute Maximum Ratings (Note)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Supply Voltages	VCC, AVCC, & PVCC	VSS-0.3		VSS+7.0	V	
Input Voltage	VIN	VSS-0.3		VSS+7.0	V	Should not exceed VCC+0.3V
Output Voltage	VOUT	VSS-0.3		VSS+7.0	V	Should not exceed VCC+0.3V
Power Dissipation	PD			600	mW	
Operating Ambient Temperature	TA	-40		+85	°C	
Storage Temperature	TSTG	-55		+150	°C	

Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Supply Voltages	VCC, AVCC, & PVCC	4.5	5.0	5.5	V	Active operation range
		3.5		6.0	V	Standby operation range
	VSS, AVSS, & PVSS		0			
Input High Voltage	VIH	0.75•VCC		VCC+0.3	V	K-Port, SI, AN0-AN2, FM, AM, $\overline{TEST}$
	VIHS	0.8•VCC		VCC+0.3	V	EX, START, $\overline{IRQ}$, $\overline{TC}$, $\overline{RESET}$
Input Low Voltage	VIL	VSS-0.3		0.25·VCC	V	K-Port, SI, AN0-AN2, FM, AM, $\overline{TEST}$
	VILS	VSS-0.3		0.2·VCC	V	EX, START, $\overline{IRQ}$, $\overline{TC}$, $\overline{RESET}$
Operating Ambient Temperature	TA	-40		+85	°C	

Note:
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Parameters (Recommended Operating Conditions Unless Otherwise Noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min	Typ	Max	
Output High Voltage	VOH	P-, R-Ports (Standard pull-up)	VCC=4.5V IOH=-200 μA	2.4			V
			VCC=4.5V IOH=-10 μA	4.0			V
Output Low Voltage	VOL	P-,R-Ports (All output options)	VCC=4,5V IOL=1.8mA			0.4	V
			VCC=4.5V IOL=3.6mA			0.6	V
Common Output Voltage	VOHC	COM0, COM1	VCC=4.5V IOHC=-100 μA	4.1			V
	VOMC		VCC=4.5 to 5.5V	1/2·VCC-0.1	1/2·VCC	1/2·VCC+0.1	V
	VOLC		VCC=4.5V IOLC=100 μA			0.4	V

DC Parameters (Cont'd)

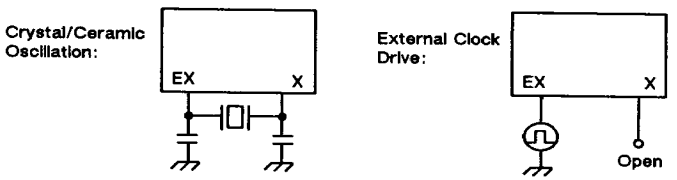
Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min	Typ	Max	
Segment Output Voltage	VOHS	SEG0-SEG25	VCC=4.5V, IOHS=-20 μA	4.1			V
	VOLS		VCC=4.5V IOLS=20 μA			0.4	V
Input Leakage Current	IIH	START, EX	VCC=5.5V VIH=5.5V			60	μA
	IIL	EX, $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{TC}}$, K-Port	VCC=5.5V VIL=0.4V			-60	μA
		R-Port (Standard pullup)	VCC=5.5V VIL=0.4V			-1.8	mA
Open-Drain Output Leakage Current	ILEAK	P-, R-Ports (Standard open-drain)	VCC=5.5V VOH=5.5V		0.1	10	μA
High Impedance I/O Leakage Current	Σ IIZ	P-, R-Ports $\overline{\text{TC}}$ (High-Z during standby mode)	VCC=6.0V VIN=0V to 6.0V (Standby mode)			± 10	μA
Supply Current	ICC	VCC	VCC=5.0V(Typ), 5.5V (Max) fc=4.5MHz (Operation) All outputs open		2	4	mA
	ICCH	VCC (Standby mode)	VCC=6.0V fc=0 (Standby) All outputs open			10	μA
	IA	AVCC	AVCC=5.0V (Typ), 5.5V (Max) fc=4.5MHz (Operation) All outputs open		1	1.5	mA
	IAH	AVCC (Standby mode)	AVCC=6.0V fc=0 (Standby mode) All outputs open			10	μA
	IP	PVCC	PVCC=5.0V (Typ), 5.5V(Max) fc=4.5MHz (Operation) All outputs open		14	22	mA
	IPH	PVCC (Standby mode)	PVCC=6.0V (Max) fc=0 (Standby) All outputs open			10	μA
Operating Frequency	f_{AML}	AM	AM direct divider mode: PVCC=4.5 to 5.5V VIN=0.5Vp-p	0.59		10	MHz
	f_{AMH}	AM	AM pulse swallow divider mode: PVCC=4.5 to 5.5V VIN=0.3Vp-p	10		32	MHz
	f_{FM}	FM	FM pulse swallow divider mode: PVCC=4.5 to 5.5V VIN=0.4Vp-p	65		120	MHz
Frame Period	t_{Fr}	COM0, COM1 SEG0 to SEG25	fc=4.5MHz		20		ms
Input Capacitance	C_{IN}	All pins except VCC, VSS, COM0, COM1, & SEG0-SEG25	fc=1MHz		10	20	pF

AC Parameters
(Recommended operating conditions unless otherwise noted.)

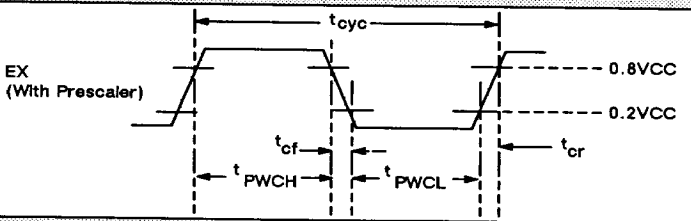
Clock Parameters

Parameter	Symbol	Pin/Port	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock Frequency	f_c	EX, X	Crystal/ceramic Osc or external clock drive.		4.5		MHz	With prescaler
Clock Cycle Time	t_{cyc}	EX, X			222		ns	
Input Clock Pulse Width	t_{PWCH}, t_{PWCL}	EX	External clock drive (with X open).	80			ns	With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open).			200	ns	

Clock Circuit Configurations



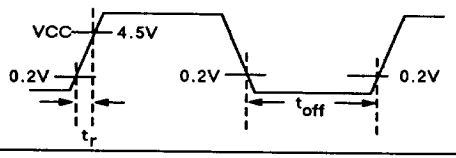
Clock Timing



Power-On Reset Parameters

Parameter	Symbol	Unit	Value			Remarks
			Min	Typ	Max	
Power Supply Rise Time	t_r	ms	0.05		50	Required for operation of the power-on reset circuit
Power Supply Shut-off Time	t_{off}	ms	1			Required for accurate circuit operation repeatability

Power-On Reset Timing



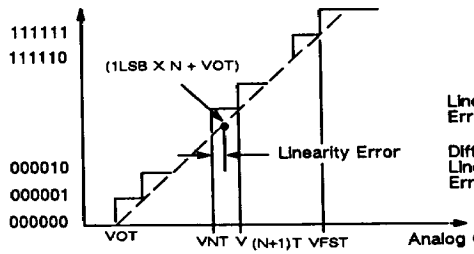
Note:
Power from a specified minimum to a specified maximum should be smoothly advanced with no abrupt changes.

AC Parameters (Cont'd)

A/D Converter Parameters[1]

Parameter	Symbol	Pin	Conditions	Value Min	Value Typ	Value Max	Unit
Resolution [2]						6	Bit
Linearity Error [3]			TA = 25°C AVCC = 5.0V			± 1.0	LSB
Differential Linearity Error [4]						± 0.9	LSB
Zero Transition Voltage	VOT			-21	+39	+99	mV
Full-Scale Transition Voltage	VFST			+4813	+4883	+4953	mV
Conversion Time			8 instructions x t_{cyc}			53.3	µs
Analog Port Input Current	IAIN	AN0-2				5	µA
Analog Input Voltage		AN0-2		0		5	V
Supply Current	IA	AVCC-AVSS	AVCC = 5.0V		1		mA

A/D Transfer Characteristics



$$1LSB = \frac{VFST - VOT}{62}$$

$$\text{Linearity Error} = \frac{VNT - (1\ LSB \times N + VOT)}{1\ LSB}\ (LSB)$$

$$\text{Differential Linearity Error} = \frac{V(N+1)T - VNT}{1\ LSB} - 1\ (LSB)$$

Notes:

1. Error between analog inputs is within 1/2 LSB.
2. **Resolution.** The minimum variation in an analog signal that can be discriminated by the A/D converter. (An analog voltage can be divided into 2^6 = 64 parts.)
3. **Linearity error.** The difference between the line connecting the zero transition point of the device (000000 ⟷ 000001) with the full scale transition point (111111 ⟷ 111110).
4. **Differential linearity error.** The difference between the ideal input voltage and the actual input voltage required to change the output voltage code by "1" LSB.

ELECTRICAL CHARACTERISTICS MB88562

Absolute Maximum Ratings (Note)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Supply Voltage	VCC, PVCC	VSS-0.3		VSS+7.0	V	
	SEGVCC	VSS-0.3		VSS+15.0	V	
Input Voltage	VIN	VSS-0.3		VSS+7.0	V	Should not exceed VCC+0.3V
Output Voltage	VOUT	VSS-0.3		VSS+7.0	V	Should not exceed VCC+0.3V
Power Dissipation	PD			600	mW	
Operating Ambient Temperature	TA	-40		+85	°C	
Storage Temperature	TSTG	-55		+150	°C	

Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Supply Voltage	VCC, PVCC	4.5	5.0	5.5	V	Active operation range
		3.5		6.0	V	Standby operation range
Segment output supply voltage	SEGVCC	11.5	12.0	12.5	V	Active operation range
Input High Voltage	VIH	0.75 •VCC		VCC+0.3	V	K-Port, SI, AN0-AN2, FM, AM, $\overline{TEST}$
	VIHS	0.8 •VCC		VCC+0.3	V	EX, START, $\overline{IRQ}$, $\overline{TC}$, $\overline{RESET}$
Input Low Voltage	VIL	VSS-0.3		0.25 ·VCC	V	K-Port, SI, AN0-AN2, FM, AM, $\overline{TEST}$
	VILS	VSS-0.3		0.2 ·VCC	V	EX, START, $\overline{IRQ}$, $\overline{TC}$, $\overline{RESET}$
Operating Ambient Temperature	TA	-40		+85	°C	

Note:
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Parameters (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min	Typ	Max	
Output High Voltage	VOH	P-, R-Ports (Standard pull-up)	VCC=4.5V IOH=-200 μA	2.4			V
			VCC=4.5V IOH=-10 μA	4.0			V
Output Low Voltage	VOL	P-,R-Ports (All output options)	VCC=4,5V IOL=1.8mA			0.4	V
			VCC=4.5V IOL=3.6mA			0.6	V
Segment Output Voltage	VOHS	SEG38-SEG0	VCC=4.5V, SEGVCC=12V, IOHS= -1.0mA	11.5			V
Segment Output Leakage Current	ILEAK	SEG38-SEG0 (No pull-down resistor)	VCC=6.0V, SEGVCC=12.5V		± 0.1	± 10	μA

DC Parameters (cont'd)

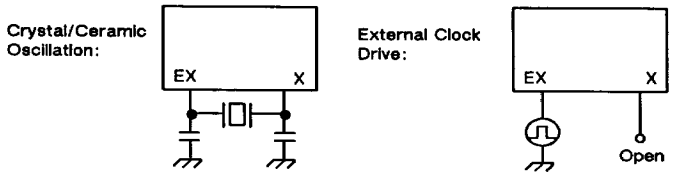
Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min	Typ	Max	
Pull-down Resistor	RL	SEG38-SEG0 (With pull-down resistor)	VCC=5.0V SEGVCC=12.0V	70		300	kΩ
Input Leakage Current	IIH	START, EX	VCC=5.5V VIH=5.5V			60	μA
	IIL	EX, $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{TC}}$, K-Port	VCC=5.5V VIL=0.4V			-60	μA
		R-Port (Standard pull-up)				-1.8	mA
Open-Drain Output Leakage Current	ILEAK	P-, R-Ports (Standard open-drain)	VCC=5.5V VOH=5.5V		0.1	10	μA
High Impedance I/O Leakage Current	Σ IIZ	P-, R-Ports $\overline{\text{TC}}$ (High-Z during standby mode)	VCC=6.0V VIN=0V to 6.0V (Standby mode)			± 10	μA
Supply Current	ICC	VCC	VCC=5.0V(Typ), 5.5V (Max) fc=4.5MHz (Operation) All outputs open		3	5.5	mA
	ICCH	VCC (Standby mode)	VCC=6.0V fc=0 (Standby) All outputs open			10	μA
	ISEG	SEGVCC	SEGVCC=12.5V VCC=5.0V fc=4.5MHz (Operation) All outputs open		5	15	mA
	IP	PVCC	PVCC=VCC=5.0V (Typ), 5.5V(Max) fc=4.5MHz (Operation) All outputs open		14	22	mA
	IPH	PVCC (Standby mode)	PVCC=VCC=6.0V (Max) fc=0 (Standby) All outputs open			10	μA
Operating Frequency	f_{AML}	AM	AM direct divider mode: PVCC=4.5 to 5.5V VIN=0.5Vp-p	0.59		10	MHz
	f_{AMH}	AM	AM pulse swallow divider mode: PVCC=4.5 to 5.5V VIN=0.3Vp-p	10		32	MHz
	f_{FM}	FM	FM pulse swallow divider mode: PVCC=4.5 to 5.5V VIN=0.4Vp-p	65		120	MHz
Input Capacitance	C_{IN}	All pins except VCC, VSS, SEG38-SEG0	fc= 1MHz		10	20	pF

AC Parameters
(Recommended operating conditions unless otherwise noted.)

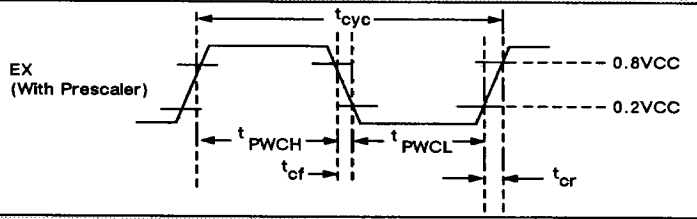
Clock Parameters

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock Frequency	f_c	EX, X	Crystal/ceramic Osc or external clock drive.		4.5		MHz	With prescaler
Clock Cycle Time	t_{cyc}	EX, X			222		ns	
Input Clock Pulse Width	t_{PWCH}, t_{PWCL}	EX	External clock drive (with X open).	80			ns	With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open).			200	ns	

Clock Circuit Configurations



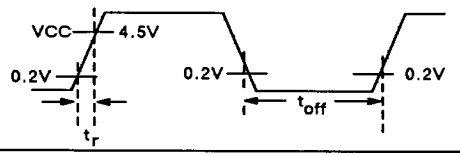
Clock Timing



Power-On Reset Parameters

Parameter	Symbol	Unit	Value			Remarks
			Min	Typ	Max	
Power Supply Rise Time	t_r	ns	0.05		50	Required for operation of the power-on reset circuit
Power Supply Shut-off Time	t_{off}	ns	1			Required for accurate circuit operation repeatability

Power-On Reset Timing



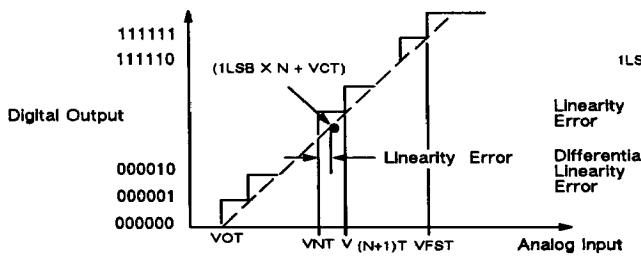
Note:
Power from a specified minimum to a specified maximum should be smoothly advanced with no abrupt changes.

2

AC Parameters (Cont'd)

A/D Converter Parameters[1]							
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Resolution [2]						6	Bit
Linearity Error [3]			TA = 25° C AVCC = 5.0V			± 1.0	LSB
Differential Linearity Error [4]						± 0.9	LSB
Zero Transition Voltage	VOT			-21	+39	+99	mV
Full-Scale Transition Voltage	VFST			+4813	+4883	+4953	mV
Conversion Time			8 instructions x t_{cyc}			53.3	µs
Analog Port Input Current	IAIN	AN0-2				5	µA
Analog Input Voltage		AN0-2		0		5	V

A/D Transfer Characteristics



$$1LSB = \frac{VFST-VOT}{62}$$

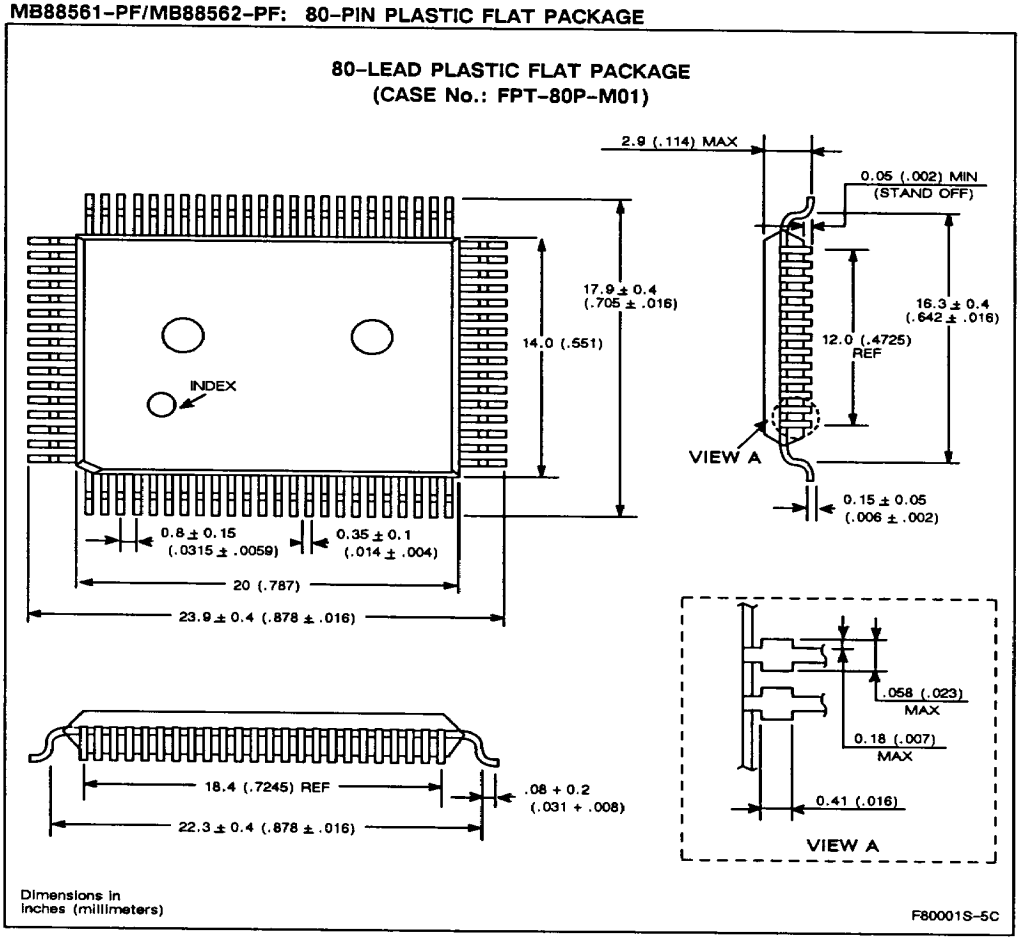
$$\text{Linearity Error} = \frac{VNT - (1\ LSB \times N+VOT)}{1\ LSB}\ (LSB)$$

$$\text{Differential Linearity Error} = \frac{V(N+1)T - VNT}{1\ LSB} - 1\ (LSB)$$

Notes:
1. Error between analog inputs is within 1/2 LSB.
2. Resolution. The minimum variation in an analog signal that can be discriminated by the A/D converter. (An analog voltage can be divided into 2^6 = 64 parts.)
3. Linearity error. The difference between the line connecting the zero transition point of the device (000000 ⟷ 000001) with the full scale transition point (111111 ⟷ 111110).
4. Differential linearity error. The difference between the ideal input voltage and the actual input voltage required to change the output voltage code by "1" LSB.

PACKAGE DIMENSIONS

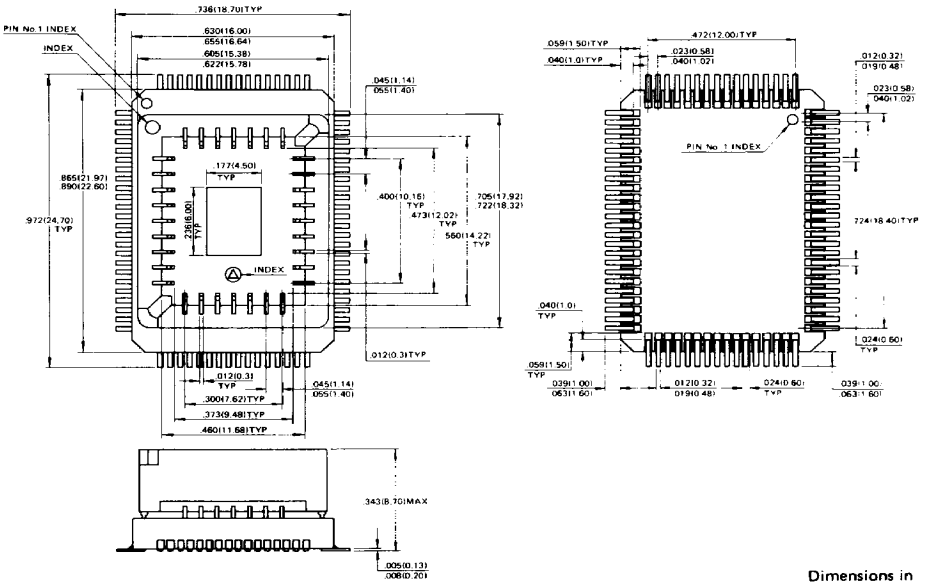
MB88561-PF/MB88562-PF: 80-PIN PLASTIC FLAT PACKAGE



PACKAGE DIMENSIONS

MB88PG561-CF/MB88PG562-CF: 80-PIN CERAMIC MULTI FLAT PACKAGE

80-LEAD QUAD IN-LINE FLAT PACKAGE MODULE
(Module No.: MQP-80C-P01)



Dimensions in inches (millimeters)