

TC5064BP, TC5065BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

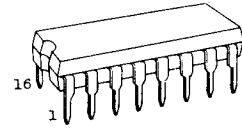
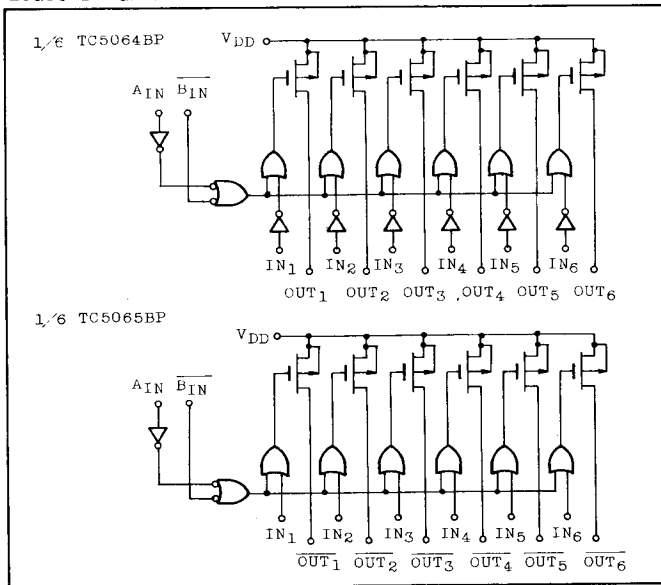
TC5064BP HEX HIGH VOLTAGE BUFFER WITH INHIBIT/NON INVERTING TYPE
TC5065BP HEX HIGH VOLTAGE BUFFER WITH INHIBIT/INVERTING TYPE

TC5064BP and TC5065BP contain six circuits of buffers having two common INHIBIT inputs ($\overline{A_{IN}}$, $\overline{B_{IN}}$). As both have the output of open drain structure with high breakdown voltage P-channel MOS FET (-50 volts... Maximum Rating), these are suitable for driving fluorescent display tubes and for interfacing with high voltage MOS LSI's. TC5064BP is non-inverting type and TC5065BP is inverting type.

ABSOLUTE MAXIMUM RATINGS

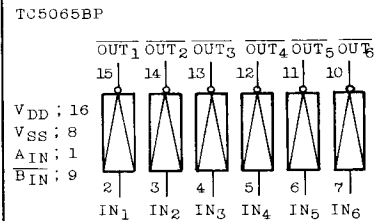
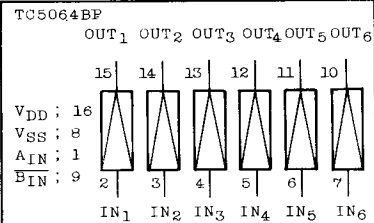
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD}	V _{VSS} -0.5 ~ V _{VSS} +20	V
Input Voltage	V _{IN}	V _{VSS} -0.5 ~ V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{DD} -50 ~ V _{DD} +0.5	V
Power Dissipation	P _D	300	mW
DC Input Current	I _{IN}	±10	mA
Storage Temperature Range	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C · 10sec	

LOGIC DIAGRAM



DIP 16 (3D16A-P)

PIN ASSIGNMENT



TRUTH TABLE

INPUT			OUTPUT	
A _{IN}	$\overline{B_{IN}}$	IN	TC5064BP	TC5065BP
L	H	L	HZ	H
L	H	H	H	HZ
*	L	*	HZ	HZ
H	*	*	HZ	HZ

HZ ; High Impedance
* ; Don't care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD}	3		18	V
Input Voltage	V _{IN}	0		V _{DD}	V
Operating Temp.	T _{opr}	-40		85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V _{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V _{OH}	I _{OUT} < 1μA V _{IN} =V _{SS} or V _{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
High Level Output Current	I _{OH}	V _{OH} =3V (V _{DD} -2V) V _{OH} =2V (V _{DD} -3V) V _{OH} =7V (V _{DD} -3V) V _{OH} =12V (V _{DD} -3V)	5	-6	-	-5	-10	-	-4	-	mA
			5	-9	-	-8	-13	-	-6	-	
			10	-12	-	-10	-25	-	-8	-	
			15	-17	-	-15	-35	-	-12	-	
High Level Input Voltage	* V _{IH}	V _{OUT} =0.5V, 4.5V V _{OUT} =1.0V, 9.0V V _{OUT} =1.5V, 13.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.5	-	
Low Level Input Voltage	* V _{IL}	V _{OUT} =0.5V, 4.5V V _{OUT} =1.0V, 9.0V V _{OUT} =1.5V, 13.5V	5	-	1.5	-	2.25	1.5	-	1.5	V
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
Output OFF Current	I _{OFF}	V _{OUT} = 0V V _{OUT} = V _{DD} -45V	15	-	-3	-	-0.01	-3	-	-10	μA
			15	-	-10	-	-1	-10	-	-20	
Input Current	I _{IH}	V _{IH} = 18V	18	-	0.3	-	10 ⁻⁵	0.3	-	1.0	μA
	I _{IL}	V _{IL} = 0V	18	-	-0.3	-	-10 ⁻⁵	-0.3	-	-1.0	
Quiescent Supply Current	I _{DD}	V _{IN} =V _{SS} , V _{DD} , OUTPUTS OPEN	5	-	4.0	-	0.005	4.0	-	30	μA
			10	-	8.0	-	0.010	8.0	-	60	
			15	-	16.0	-	0.015	16.0	-	120	

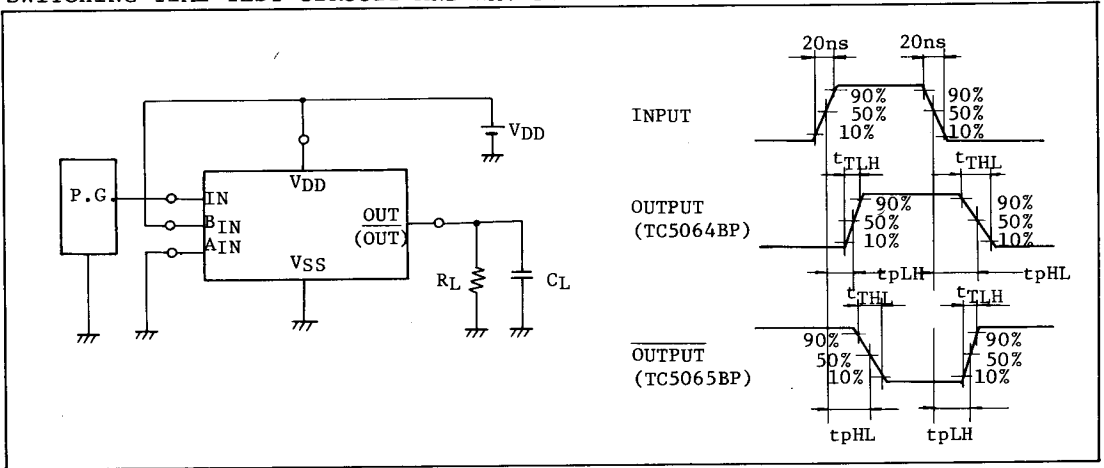
* R_L = 20 kΩ

SWITCHING CHARACTERISTICS (T_a=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t _{TLH}	R _L = 20 kΩ	5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	
Output Fall Time	t _{THL}	R _L = 20 kΩ	5	-	5.0	8.0	μs
			10	-	5.0	8.0	
			15	-	5.0	8.0	
(LOW-HIGH) Propagation Delay Time	t _{pLH}	R _L = 20 kΩ	5	-	200	500	ns
			10	-	100	250	
			15	-	80	200	
(HIGH-LOW) Propagation Delay Time	t _{pHL}	R _L = 20 kΩ	5	-	2.0	4.0	μs
			10	-	2.0	4.0	
			15	-	2.0	4.0	
Input Capacity	C _{IN}			5	7.5	pF	

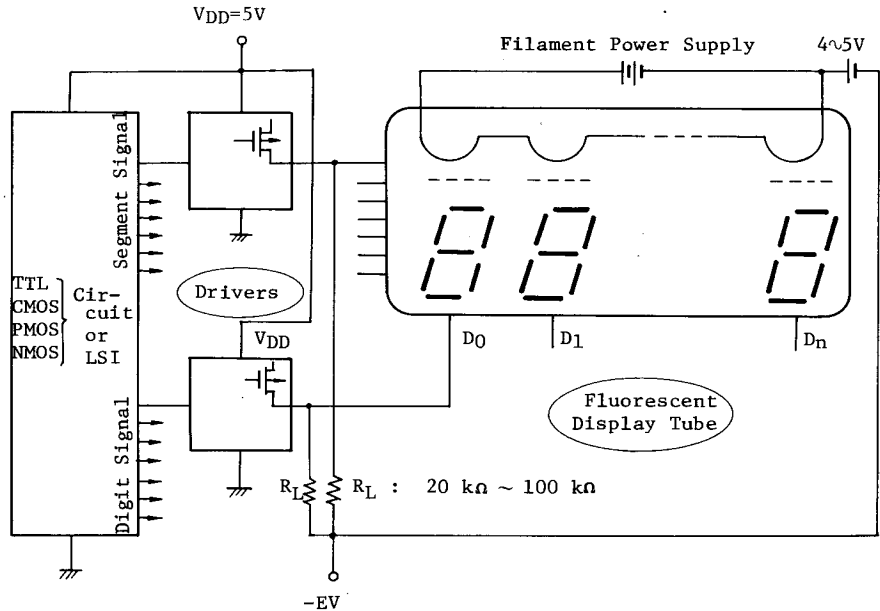
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SWITCHING TIME TEST CIRCUIT AND WAVEFORM



EXAMPLES OF APPLICABLE CIRCUITS

(1) Fluorescent Display Tube Driving Circuit



(2) Interface between CMOS and PMOS

