256 WORD x 4 BIT CMOS RAM

TC5501P/-1
TC5501D/-1

DESCRIPTION

The TC5501P/D is a fully static read write memory organized as 256 words by 4 bits using CMOS technology. Because of ultra low power dissipation, the TC5501P/D can be used as battery operated portable memory system and also as a nonvolatile memory with battery back up. The TC5501P/D operates from a single 5V power supply with a static operation, so that the no refresh periods are required. This simplifies the power supply circuit design.

The three state outputs simplify the memory expansion making the TC5501P/D suitable for use in a microprocessor peripheral memory. Since the minimum data retention voltage is 2V, the battery back up system needs only simple circuit. By using Toshiba's original C^2MOS technology, the device circuitry is not only simplified but wide operating margin and noise margin are also realized.

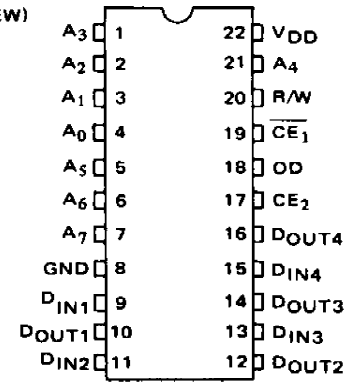
The TC5501P/D is offered in standard 22 pin plastic and cerdip packages, 0.4 inch in width.

FEATURES

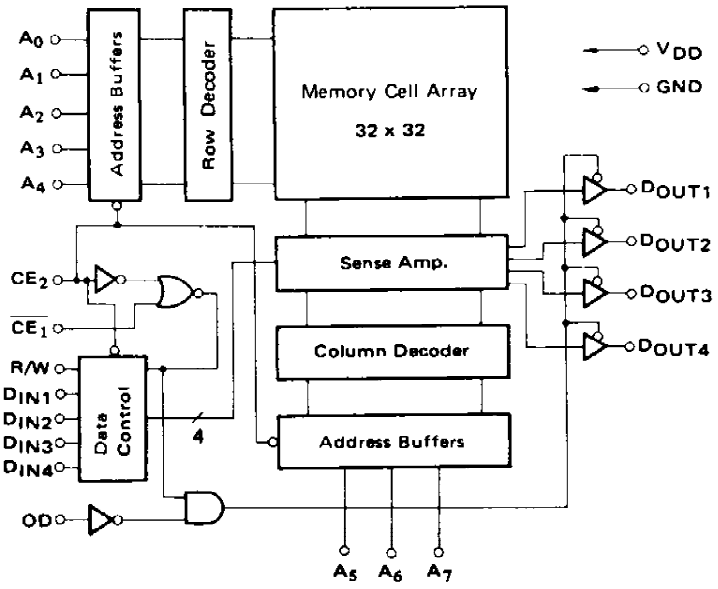
- Low Power Dissipation
  - 55μW (MAX.) STANDBY
  - 83mW (MAX.) OPERATING
- Single 5V Power Supply
- Data Retention Voltage 2V to 5.5V
- Package
  - Plastic DIP : TC5501P
  - Cerdip DIP : TC5501D
- Fully static operation
- Three State Output
- Input/output, TTL Compatible
- Access Time
  TC5501P/D ; $t_{ACC} \leqq 450$ns (MAX.)
  TC5501P-1/D-1; $t_{ACC} \leqq 650$ns (MAX.)

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_7$	Address Inputs
R/W	Read Write Input
$\overline{CE_1}$, CE_2	Chip Enable Inputs
$D_{IN1 \sim 4}$	Data Inputs
$D_{OUT1 \sim 4}$	Data Outputs
OD	Output Disable Input
V_{DD}/GND	Power Supply Terminals

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3 ~ V_{DD} + 0.3	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation (Ta = 85°C)	800	mW
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{OPR}	Operating Temperature	−30 ~ 85	°C

DC RECOMMENDED OPERATING CONDITION

SYMBOL	PARAMETER	MIN	TYP.	MAX.	UNITS
V_{DD}	Power Supply Voltage	4.5	–	5.5	V
V_{IH}	Input High Level Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Level Voltage	-0.3	–	0.65	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

DC CHARACTERISTICS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP(1)	MAX.	UNITS
I_{IN}	Input Current	$0 \leqq V_{IN} \leqq V_{DD}$	–	±0.05	±1.0	μA
I_{DDS}	Standby Current	V_{DD} = 2.0V to 5.5V CE_2 = 0.2V, Output open	–	0.2	10	μA
I_{DDO}	Operating Current	V_{DD} = 5.5V, t_{CYC} = 1μs	–	6.2	15	mA
I_{LO}	Output Leakage Current	$0 \leqq V_{OUT} \leqq V_{DD}$	–	±0.05	±1.0	μA
I_{OH}	Output High Current	V_{DD} = 4.5V, V_{OH} = 2.4V	−1.0	−2.0	–	mA
I_{OL}	Output Low Current	V_{DD} = 4.5V, V_{OL} = 0.4V	2.0	3.0	–	mA

Note (1) Ta = 25°C V_{DD} = 5V

CAPACITANCE (2) (Ta = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1MHz	–	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1MHz	–	7	15	pF

Note (2) This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

- **READ CYCLE**

SYMBOL	PARAMETER	TC5501P/D		TC5501P-1/D-1		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	450	–	650	–	ns
t_{ACC}	Address Access Time	–	450	–	650	ns
t_{ACC1}	$\overline{CE}_1$ Access Time	–	400	–	600	ns
t_{ACC2}	CE_2 Access Time	–	500	–	700	ns
t_{OD0}	OD Access Time	–	250	–	350	ns
t_{COE}	Output Enable Time	0	–	0	–	ns
t_{DIS}	Output Disable Time	0	130	0	150	ns
t_{OH}	Output Data Hold Time	0	–	0	–	ns

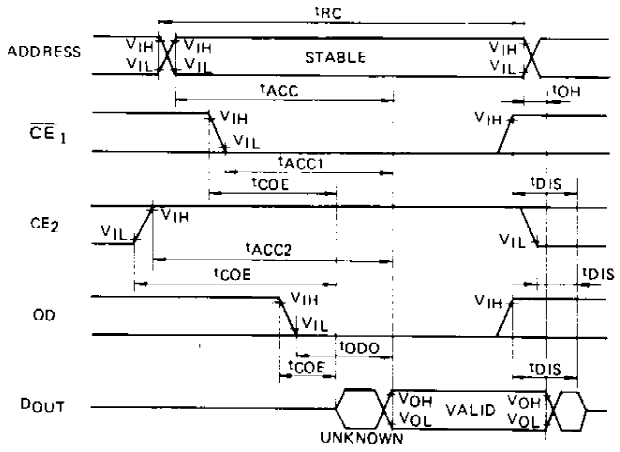
- **WRITE CYCLE**

SYMBOL	PARAMETER	TC5501P/D		TC5501P-1/D-1		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	450	–	650	–	ns
t_{AW}	Address Setup Time	130	–	150	–	ns
t_{CW}	CE_2 Setup Time	130	–	150	–	ns
t_{WP}	Write Pulse Width	250	–	400	–	ns
t_{DS}	Data Setup Time	250	–	400	–	ns
t_{DH}	Data Hold Time	50	–	100	–	ns
t_{WR}	Write Recovery Time	50	–	50	–	ns

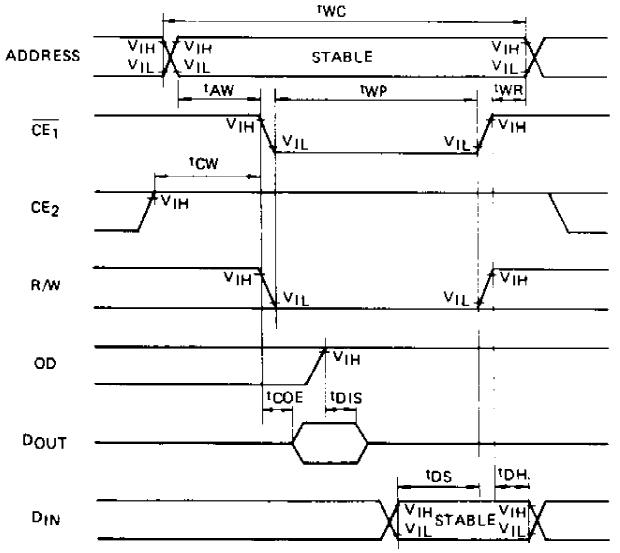
A.C. TEST CONDITIONS

- Output Load : 100 pF + 1 TTL Gate
- Input Pulse Levels : 0.45V, 2.4V
- Timing Measurement Reference Levels
  - Input : 0.65V, 2.2V
  - Output : 0.65V, 2.2V
- Input Pulse Rise and Fall Times : 10ns

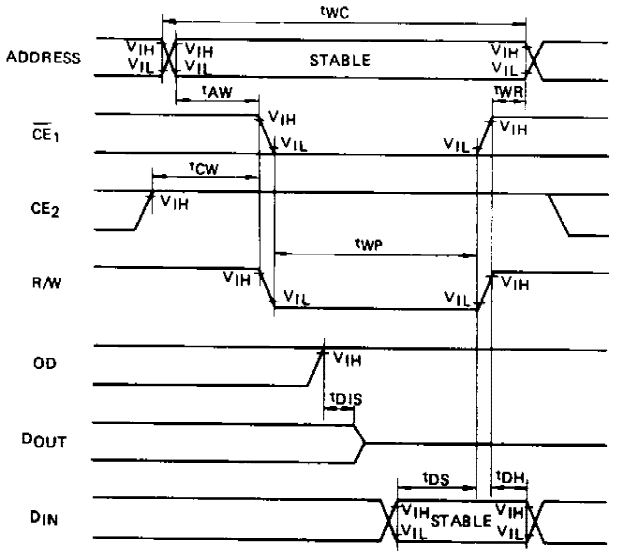
Read Cycle



Write Cycle 1

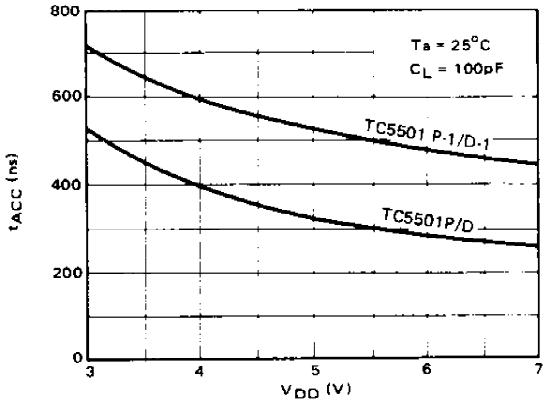


Write Cycle 2

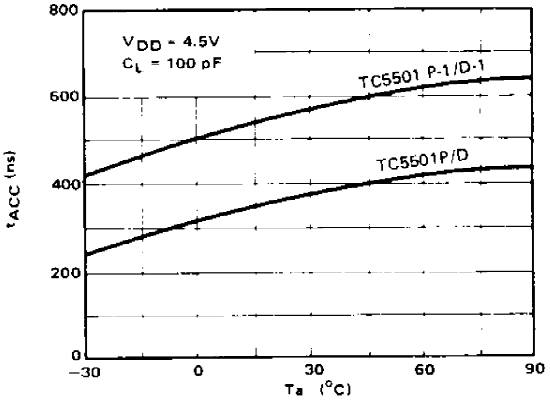


TYPICAL CHARACTERISTICS

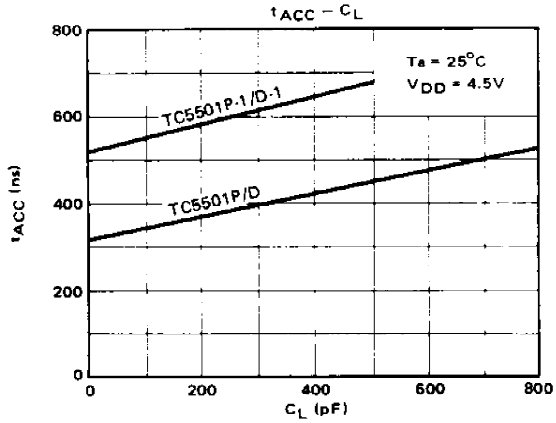
t_{ACC} – V_{DD}



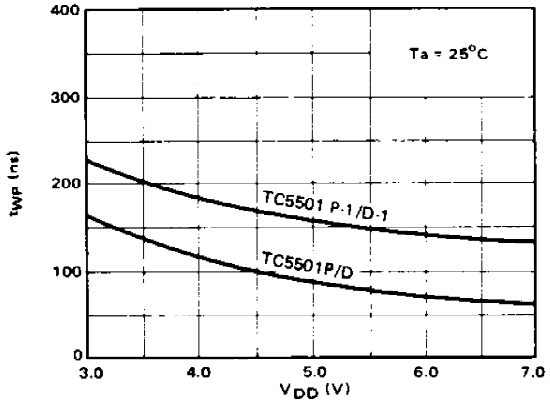
t_{ACC} – Ta



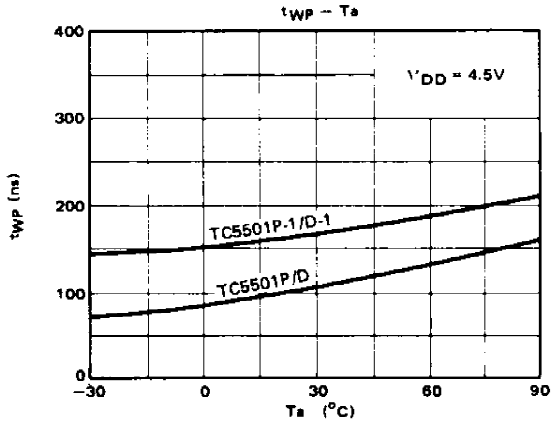
t_{ACC} – C_L



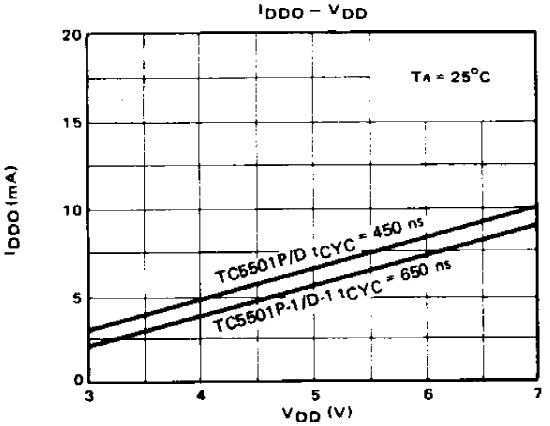
t_{WP} – V_{DD}



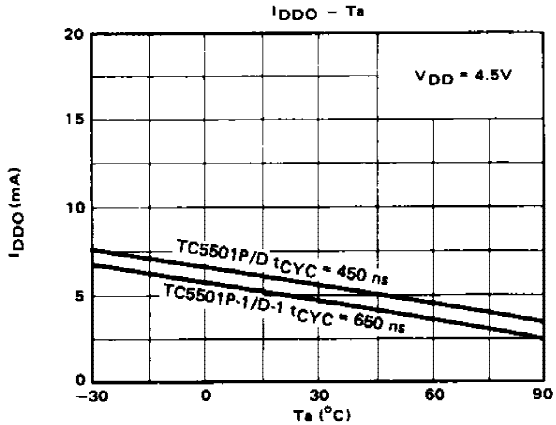
t_{WP} – Ta



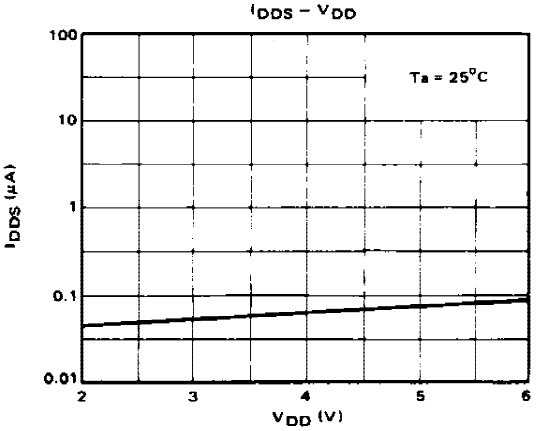
I_{DDO} – V_{DD}



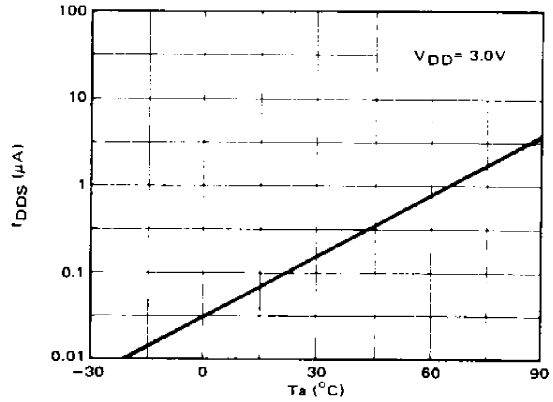
I_{DDO} – Ta



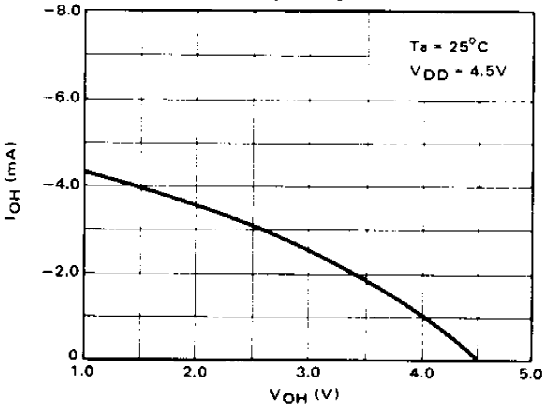
I_{DDS} – V_{DD}



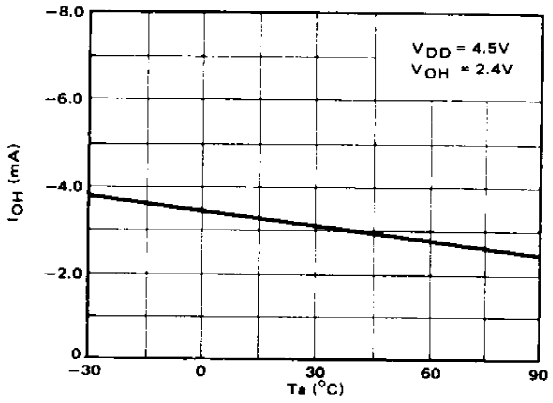
I_{DDS} – Ta



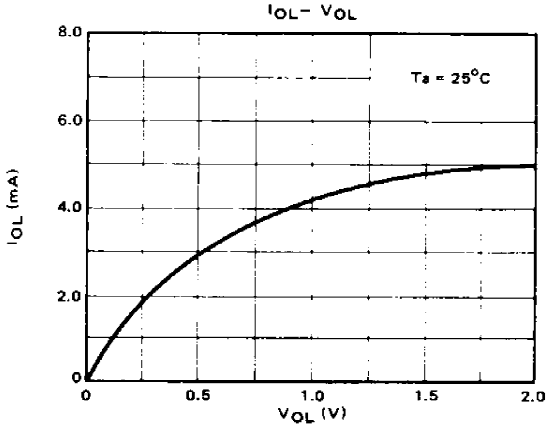
I_{OH} – V_{OH}



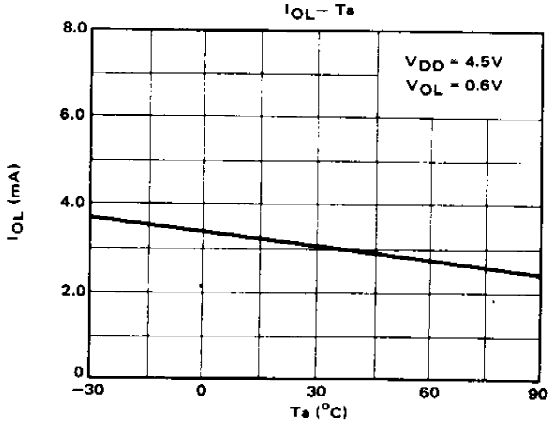
I_{OH} – Ta



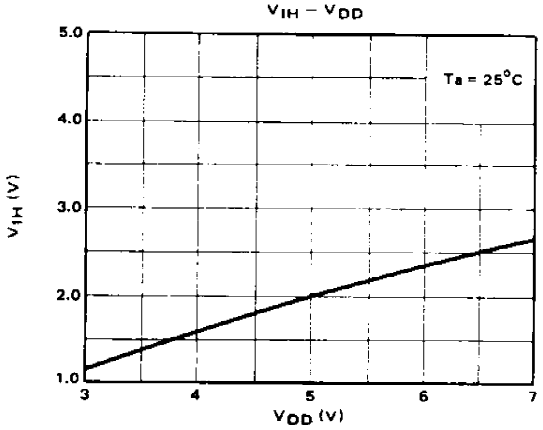
I_{OL}– V_{OL}



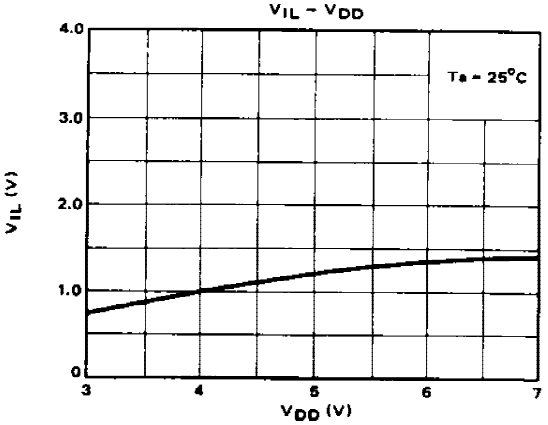
I_{OL}– Ta



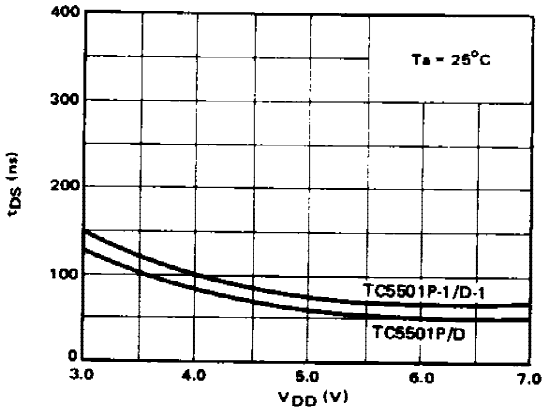
V_{IH} – V_{DD}



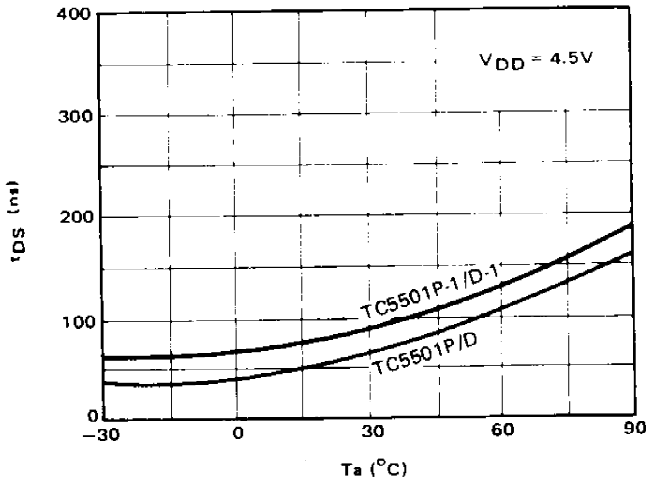
V_{IL} – V_{DD}



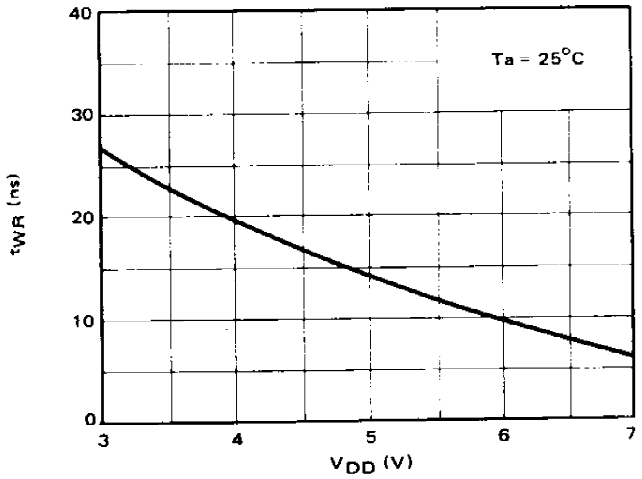
t_{DS} – V_{DD}



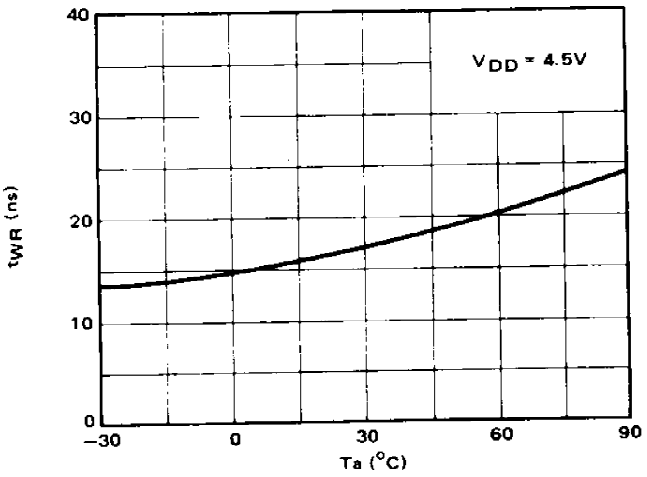
t_{DS} – Ta



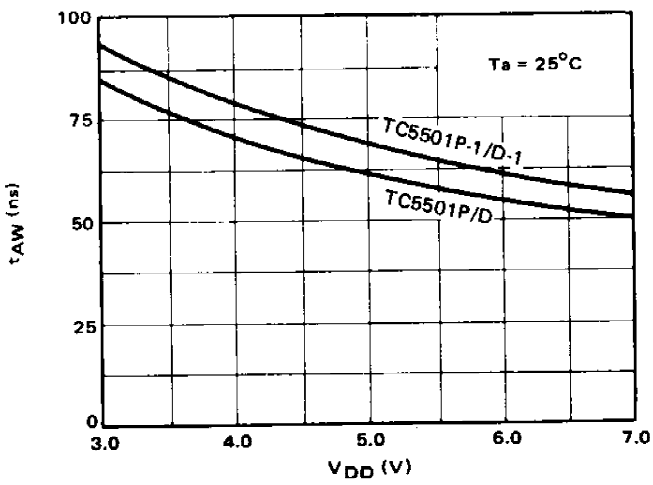
t_{WR} – V_{DD}



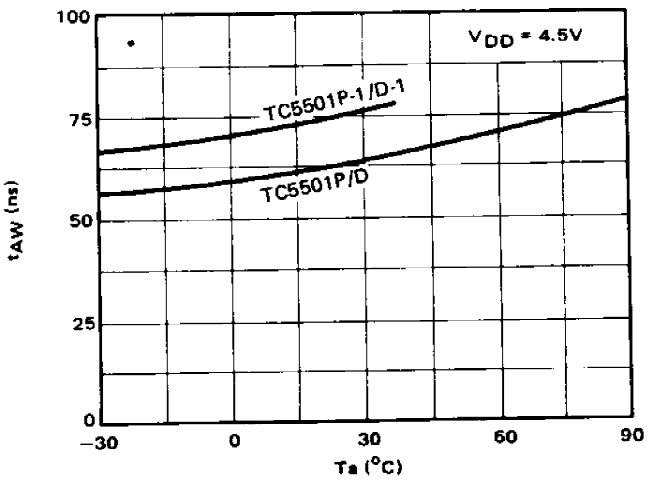
t_{WR} – Ta



t_{AW} – V_{DD}



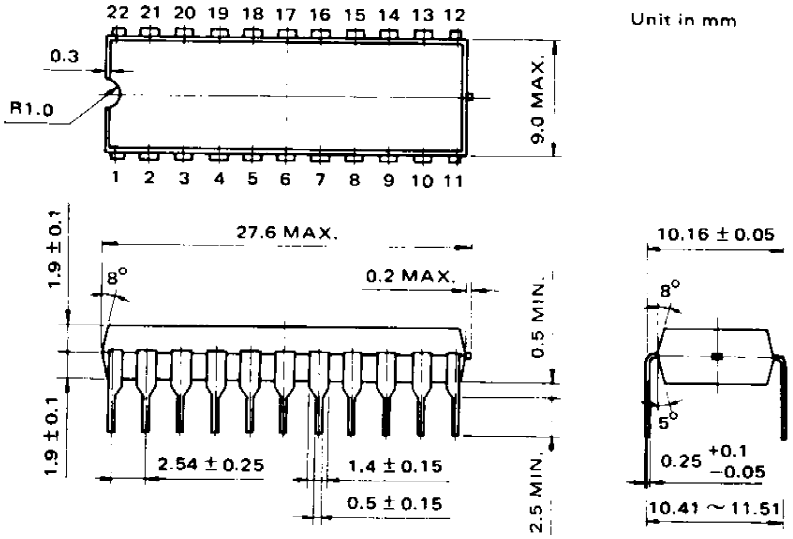
t_{AW} – Ta



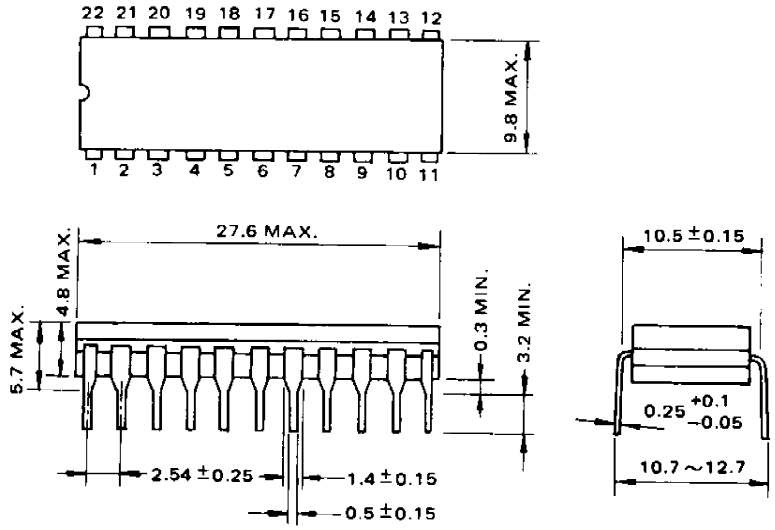
OUTLINE DRAWINGS

PLASTIC PACKAGE

Unit in mm



CERDIP PACKAGE



Notes: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 22 leads.