Toshiba 東芝

INTEGRATED CIRCUIT

TECHNICAL DATA

TC9123BP

"C²MOS" DIGITAL INTEGRATED CIRCUIT

SILICON MONOLITHIC

TENTATIVE

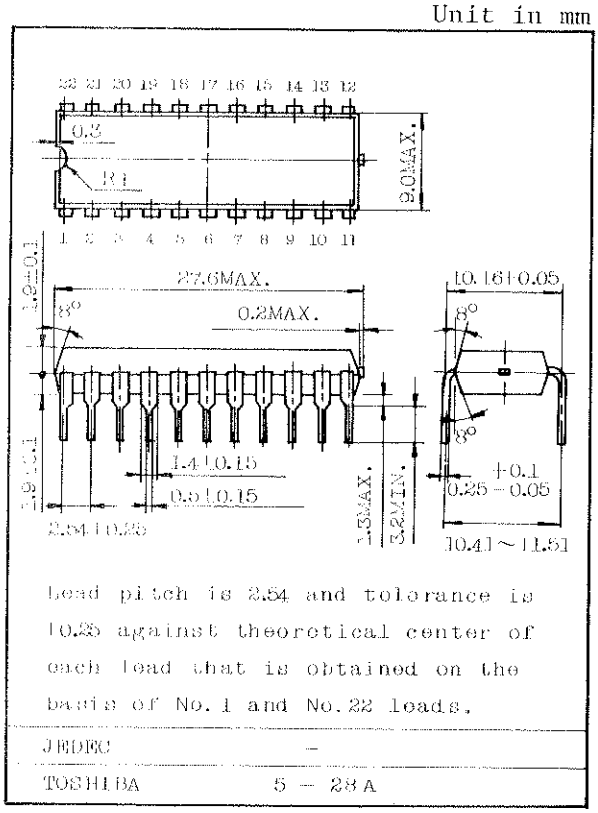
TC9123BP FM/AM SYNTHESIZER TUNER PLL

TC9123BP is C-MOS LSI newly developed as PLL for FM/AM Synthesizer Tuner and pairing with C-MOS LSI TC9124AP for control which is a different chip will make a high performance synthesizer tuner.

As seven intermediate frequencies (IF) when receiving FM signal are available around 10.7MHz with the interval of 25 kHz for TC9123BP combined with the prescaller TD6102P, it can be freely selected to match with the filter to be used.

And since the 1/8 frequency divider can be used as the prescaller when FM signal is received by improving the speed of the programmable counter, high S/N ratio can be obtained.

Unit in mm



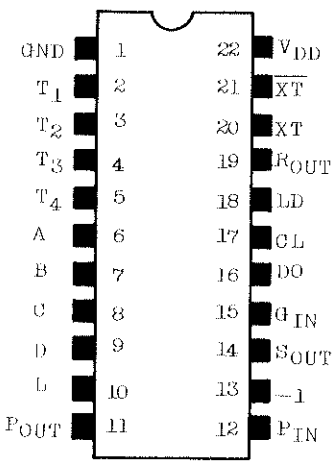
Lead pitch is 2.54 and tolorance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.22 leads.

JEDEC	—
TOSHIBA	5 − 28A

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3∿9.0	V
Input Voltage	V_{IN}	−0.3∿V_{DD}+0.3	V
Operation Temperature	T_{opr}	−30∿ 70	°C
Storage Temperature	T_{stg}	−55∿ 125	°C

PIN CONNECTION



FUNCTIONAL DESCRIPTION OF PINS

PIN NO.	SYMBOL	NAME OF PIN	DESCRIPTION OF FUNCTION AND OPERATION	REMARKS
1	GND	GND Pin		
2 3 4 5	T_1 T_2 T_3 T_4	Input pins of digit timing signals	These are digit timing input pins to designate the digits reading the program data A through D. T_1 is the least significant digit and T_4 is the most significant digit.	Equipped with pull down resistors.
6 7 8 9	A B C D	Input pins of program data	Input pins for receive mode setting data and frequency division data of the programmable counter.	Equipped with pull down resistors.
10	L	Load input pin	Input pin of read command for data A through D. When this pin is at "1" level, the data is read and when it is at "0" level, the previous data is retained regardless of other inputs.	Equipped with pull down resistors
11	Pout	Output pin of programable counter	Pin for the programable counter frequency division output. This is connected to the prescaller for IF adjustment or for 150K shift of FME mode.	
12	PIN	Input pin of programable counter	Input pin of programable counter.	Equipped with amplifier
13	- 1	Input pin of frequency division shift command	When this pin is grounded, the frequency division of the programable counter is shifted by -1 from the programmed value. (Activated only in FM mode)	Equipped with pull up resistors

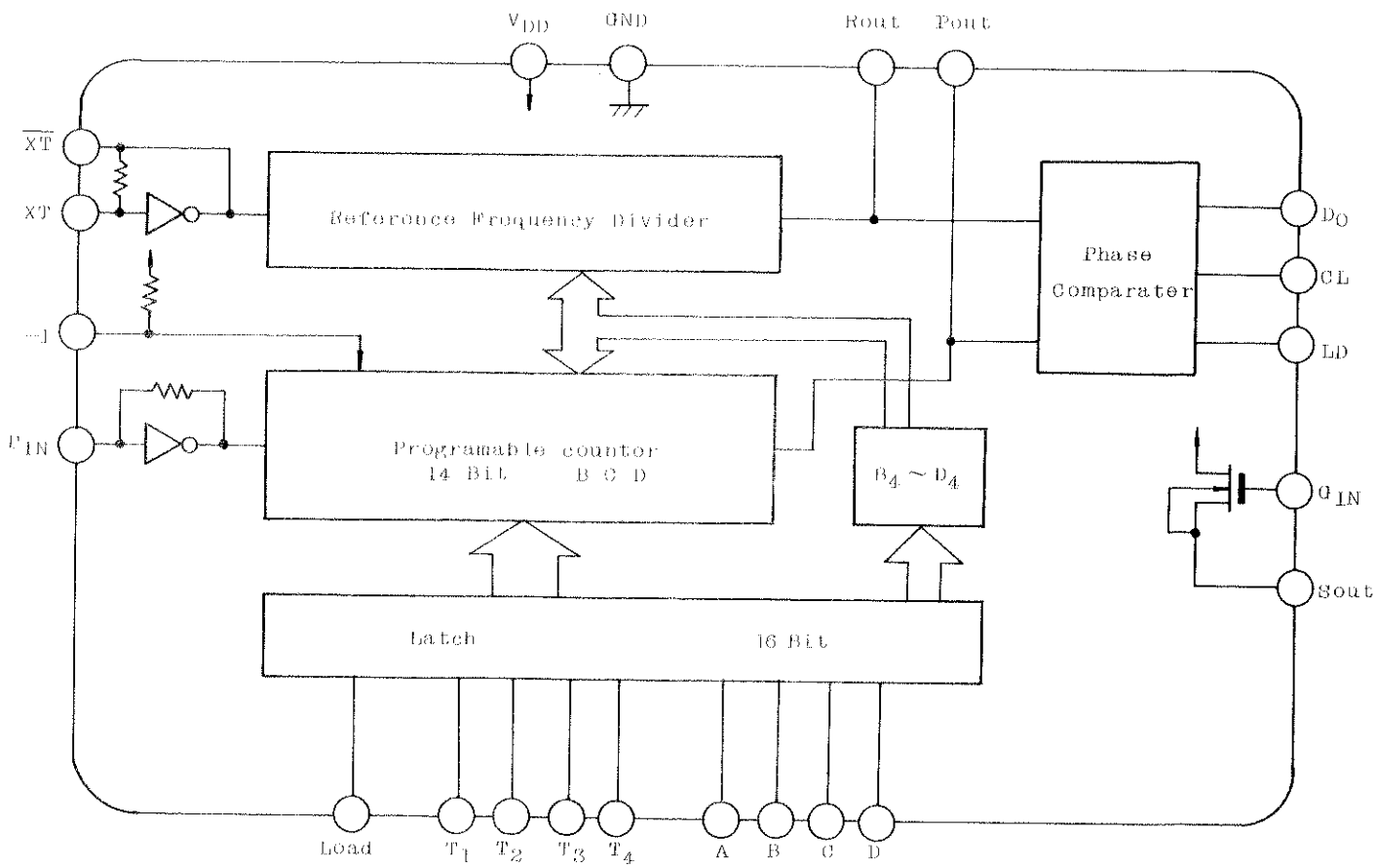
PIN NO.	SYMBOL	NAME OF PIN	DESCRIPTION OF FUNCTION AND OPERATION	REMARKS
14 15	S_{out} GIN	FET pins for low pass filter	Gate input and source output pins of source follower N channel MOS FET used in the low pass filter amplifier.	
16 17 18	D_O C_L LD	Output pins of phase comparator	Output pin of phase comparator, which is connected to the low pass filter. Pin for connecting external CR which sets the time constant of lock out detection. Lock out output pin which becomes "L" during lock out.	
19	R_{out}	Reference frequency output pin	Reference frequency output which provides 12.5 kHz for FM and 1 kHz for AM.	
20 21	XT $\overline{XT}$	Pins for crystal oscillator	Pin to connect 6.4 MHz crystal oscillator.	Equipped with feed-back resistor.
22	V_{DD}	Power supply pin	8 ± 0.5 volts for FMu, 7.0∿8.5 volts for FM_L	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified V_{DD}=7.5V, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage	V_{DD}				7 ∿ 9.5			V
Operating Power Supply Current	I_{DD}(1)		6.40MHz X-tal Connected to X_T - $\overline{X_T}$,	P_{IN}=10MHz	-	12	20	mA
	I_{DD}(2)			P_{IN}=16MHz	-	17	25	
PROGRAMABLE COUNTER								
Max. Operating Frequency	f_{MAX}		V_{IN}=1.7Vp-p Note 1	V_{DD}=7V	16	-	-	MHz
Min. Operating Frequency	f_{MIN}		V_{IN}=1.7Vp-p, Note 1		-	-	0.5	MHz
Min. Operating Input Voltage	$V_{IN\ MIN}$		P_{IN}=16MHz		1.7	-	-	Vp-p
REFERENCE FREQUENCY DIVIDER								
Max. Operating Frequency	f_{MAX}		Note 1, 6.4MHz X-tal connected to X_T-$\overline{X_T}$		6.4	-	-	MHz
"H" LEVEL OUTPUT CURRENT								
R_{OUT} Output	$I_{OH\ ROUT}$		V_{OH}=6.5V		-0.5	-	-	mA
P_{OUT} Output	$I_{OH\ POUT}$							
D_O Output	$I_{OH\ DO}$							
L_D Output	$I_{OH\ LD}$							
C_L Output	$I_{OH\ CL}$							
"L" LEVEL OUTPUT CURRENT								
R_{OUT} Output	$I_{OL\ ROUT}$		V_{OL}=1.0V		0.5	-	-	mA
P_{OUT} Output	$I_{OL\ POUT}$							
D_O Output	$I_{OL\ DO}$							
L_D Output	$I_{OL\ LD}$							
DC TRI-STATE LEAKAGE CURRENT								
Leakage Current	"H" Level	$I_{TLH\ DO}$	-		-	-	0.1	μA
	"L" Level	$I_{TLL\ DO}$			-	-	-0.1	
GIN INPUT LEAKAGE CURRENT								
Leakage Current	"H" Level	$I_{LLH\ GIN}$			-	-	0.1	μA
	"L" Level	$I_{TLL\ GIN}$			-	-	-0.1	
S_{OUT}								
Drain Current		I_{DS}	V_{GS}=2V		-0.5	-	-5.0	mA
T1 ∿ T4, A ∿ D, L, -1								
Pull Up/Down Resistance		R_{IN}			10	-	60	kΩ
Input Voltage	"H" Level	V_{IH}			6.0	-	V_{DD} + 0.3	V
	"L" Level	V_{IL}			-0.3	-	1.5	V

Note 1: All temperature above is Ta = -30 ∿ 70°C.

BLOCK DIAGRAM



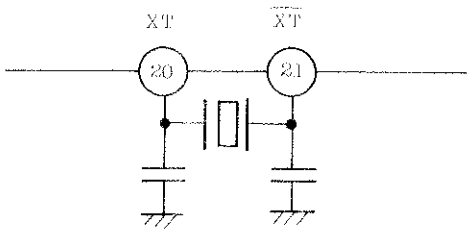
FUNCTIONAL DESCRIPTION OF EACH ELEMENT

1. REFERENCE FREQUENCY DIVIDER

1) The reference frequency divider consists of the crystal oscillator's amplifier for which 6.4 MHz X-tal is externally connected and the frequency divider which generates the reference frequencies of 12.5 kHz for FM mode and 1 kHz for AM mode by dividing the oscillator output. The division ratios are 1/512 for FM and 1/6400 for AM.

2) The divided output is fed to outside from R_{out} pin as well as fed to the reference input of phase comparator.

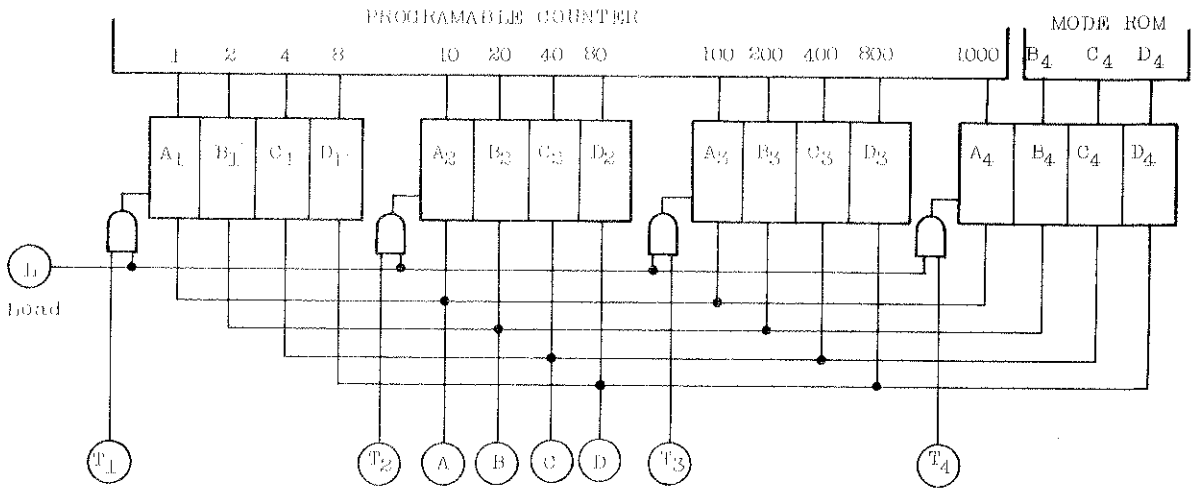
3) X-tal oscillation amplifier is equipped with bias resistor enabling to complete the circuit with simple external connection shown below.



2. PROGRAM DATA LATCHES

1) The data to set the frequency division ratio of the programable counter in the receiving mode are serially and dynamically input from four input pins A through D at the timings of four digits T_1 through T_4 in TC9123BP and stored in the latches converting to 16 bit parallel data to control the operation.

2) The configuration of data latches is as shown below.



3. PROGRAMMABLE COUNTER

1) The programable counter is the frequency divider which can control the frequency division ratio according to the program data supplied from outside and has the configuration of 3 · 1/2 BCD digits (14 bits).

2) Since the speed of program counter has been improved for TC9123BP, the 1/8 frequency divider can be used as the prescaller for receiving FM.

3) There is the frequency difference equal to the intermediate frequency between the receiving frequency and the oscillation frequency of V_{CC} (local oscillator) since the local oscillator is controlled by PLL in the receiver.

TC9123BP has the internal frequency division ratio shift function which corresponds to IF enabling to use the receiving frequency data as the program data for the programable counter and resulting simplification of total system.

The offset values of frequency division for receive mode are as follows.

NAME OF MODE	OFFSET VALUE OF FREQUENCY DIVISION
AM_1	+460
AM_2	+459
FM_L	-107
FM_U	+107

4) The frequency division output of program counter is fed to the signal input (Sin) of the phase comparator and compared with the output frequency of the reference frequency divider.

5) TC9123BP has the frequency division output terminal P_{out} of program counter and -1 terminal having the function of decrementing frequency division ratio by one for any arbitrary program data, and the prescaller TD6102P is controlled by utilizing these two terminals enabling IF fine tuning during FM receiving.
This operation is explained in detail later.

6) Since the frequency input terminal PIN of programable counter is equipped with the amplifier with self bias, input signal is supplied via capacitor coupling and proper operation can be obtained with small amplitude.

4. PHASE COMPARATOR

The phase comparator is the element which compares the phase difference between the reference frequency divider output and the programable counter output and controls VCO through the low pass filter to make the frequencies and the phases of these two signals coincide.

1) Output of DO terminal (Tri-state output of C-MOS)

a) When the phase of frequency devided output of programable counter lags behind the reference frequency, DO output is held at "L" level by turning Nch FET on during the period corresponding to the phase difference.

b) When it leads on the contrary, DO output is held at "H" level by turning Pch FET on during the period of the phase difference.

c) In neither case, DO output is placed in high impedance condition by turning both Nch and Pch off.

2) Output of CL and LD terminals

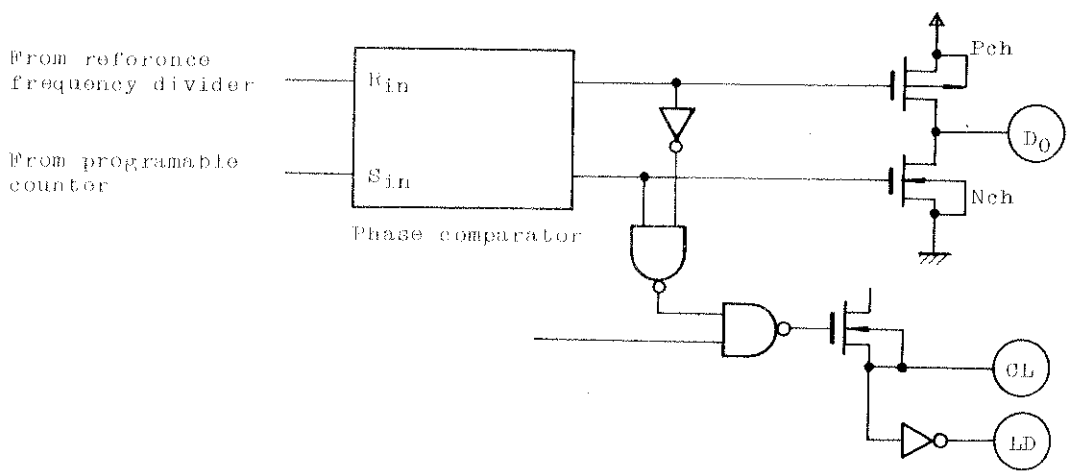
a) LD terminal is provided as a terminal to be utilized for muting, dtc by detecting unlocked operating condition of PLL loop.

b) A circuit which is activated with high sensitivity by vibration of the unit or by external noise is provided in the lockout detection circuit to detect the condition that the phase difference exceeds a specific value to prevent interruption of signal. This value of phase difference is set to ±5.6° for FM and ±1.8° for AM.

c) CL terminal is to connect CR time constant circuit externally which establishes the time period from LD terminal falling to "L" level releasing the lock to LD terminal returning to "H" level after locking the loop again.

$$T \doteqdot 0.7RC$$

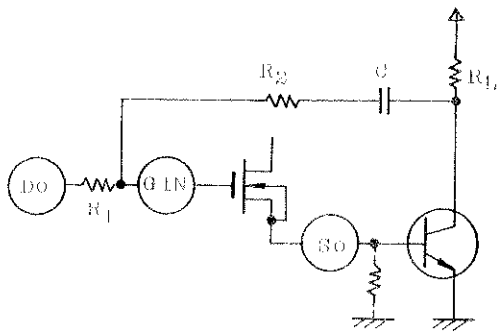
d) Schematic of phase comparator portion.



3) Source follower FET for low pass filter

a) TC 9123BP is equipped with source follower Nch MOS FET to compose the active low pass filter and has GIN (gate input) terminal and S_{out} (source output) terminal.

b) This MOS FET composes the amplifier with high input impedance externally connecting NPN transistor in Darlington configuration and MOS FET equipped is the enhancement type which provides good operating point.



RECEIVING BAND OF TC9123BP

Basically, TC9123BP has four receiving bands AM_1, AM_2, FM_L and FM_U. These receiving modes are selected by the external program and in TC9123BP, switching of phase comparison reference frequency and switching of frequency division offset value of the programable counter are performed according to the instruction.

Receiving in FME mode is also possible by mutual control with the prescaller and this will be described in separate paragraph.

1. OPERATION OF TC9123BP FOR EACH MODE

Reference frequencies and offset values of TC9123BP for the above four modes are as follows.

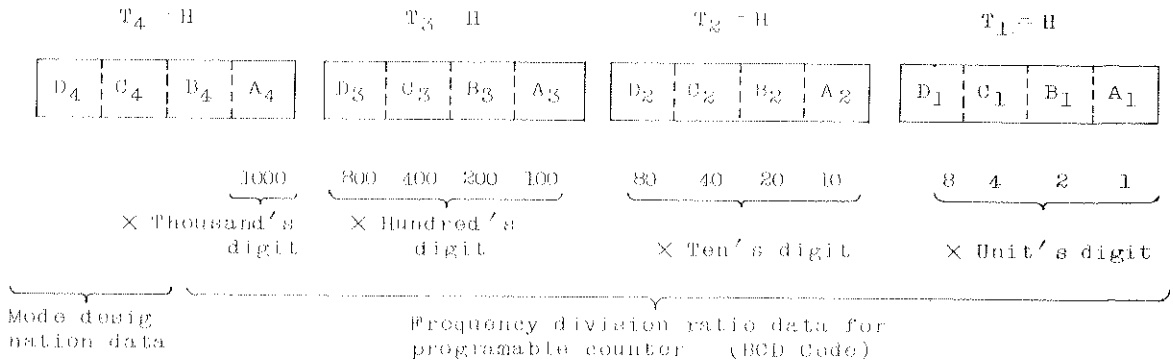
MODE	REFERENCE FREQUENCY	FREQUENCY DIVISION RATIO OF PROGRAMABLE COUNTER	REMAKRS
AM_1	1.0 kHz	N = n + 460	AM 10 kHz Step
AM_2	1.0 kHz	N = n + 459	AM 9 kHz Step
FM_L	12.5 kHz	N = n - 107	FM Japan
FM_U	12.5 kHz	N = n + 107	FM Foreign

(Note) N : Actual frequency division ratio of programable counter.
n : Programmed frequency division ratio data.

1) Since the reference frequency for FM is selected as high as 12.5 kHz, the high S/N ratio has been obtained. The prescaller for receiving FM is 1/8.
2) Having 1 kHz as the reference frequency for AM, fine adjustment of the optimum receiving condition can be achieved.

PROGRAMMING OF TC9123BP

1. The program data which specify the operation of TC9123BP contain the mode data designating FM or AM and the data designating frequency division ratio of the programable counter. All of these are dynamically programmed through four input terminals A through D.
The inputs of A through D have different meanings depending on each timing of T_1 through T_4, and are stored in the 16 bit latches after being converted internally to parallel form. The meanings of data at A through D for each timing are as follows.



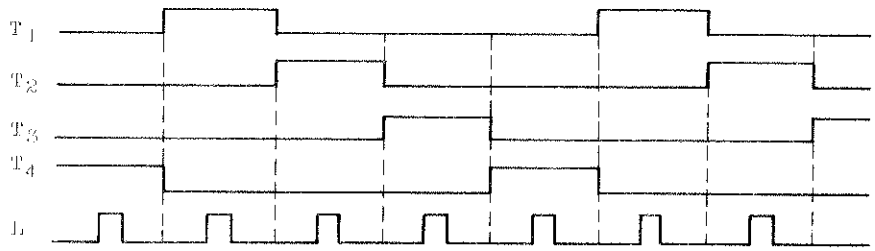
2. The operational modes by data B_4, C_4 and D_4 are as follows.

NAME OF MODE	B_4	C_4	D4
AM - 1	0	1	0
AM - 2	0	0	0
FM - L	1	0	1
FM - U	1	1	1
FM - E	1	1	1
	0	1	1

* Addition of 50 kHz in FM-E mode is performed by the coupled operation of prescaller (TD6101P or TD6102P) and TC9123BP.

3. The load signal input is the input which gives the instruction to read the data from terminals A through D. While this terminal is kept at "1" level, the data at A through D are read into the internal latch, and when it is at "0" level, the previously read data are retained without reading anything regardless of T_1 through T_4 and A through D.

In order to prevent any erroneous operations of reading data at the timing of switching $T_1 \sim T_4$ timing or switching data at A through D, it is appropriate to apply the signal shown below to the load terminal.



4. Examples of program

As examples of programming TC9123BP, the data at through D at the timing of T_1 through T_4 are illustrated for AML, 82.6 MHz and AM_2, 1251 kHz.

(1) FM_L, 82.5 MHz

T_4				T_3				T_2				T_1			
D_4	C_4	B_4	A_4	D_3	C_3	B_3	A_3	D_2	C_2	B_2	A_2	D_1	C_1	B_1	A_1
1	0	1	0	1	0	0	0	0	0	1	0	0	1	0	1

(2) AM_2, 1251 kHz

0	0	0	1	0	0	1	0	0	1	0	1	0	0	0	1

5. When TC9123BP is used as the controller of TC9123BP, proper operation can be achieved by simply connecting $T_1 \sim T_4$, A ~ D and load without paying special considerations on the programming method. All of the operational mode designations and the frequency data are controlled by TC9124AP.

FINE ADJUSTMENT OF INTERMEDIATE FREQUENCY FOR RECEIVING FM

Since IF can be freely selected from seven kinds of ±25, ±50 and ±75 (kHz) around nominal 10.7 MHz in FM mode for TC9123BP, receiving in ideal condition can be achieved compensating variety of IF filters used.

This operation is achieved by the combination of TC9123BP and prescaller TD6102P. Detail description of this method follows.

1. First of all, basic principles which must be understood prior to perform this operation are described.
   1) When P_{out} terminal of TC9123BP and +25k terminal of TD6102P are connected, the local oscillator frequency is shifted by +25 kHz.
   2) When +50k terminal is similarly connected, it is shifted by +50 kHz.
   3) If both of +25k and +50k terminals are connected, it is shifted by +75 kHz.
   4) If -1 terminal of TC9123BP is connected to GND ("G" level), the local oscillator is shifted by -100 kHz.
   5) In the case of FM_L, if the local oscillator frequency shifts by $+\Delta f$, IF becomes $10.7 - \Delta f$ and if it shifts by $-\Delta f$, IF becomes $10.7 + \Delta f$.
   6) In the case of FM_U, if the local oscillator frequency shifts by $+\Delta f$, IF becomes $10.7 + \Delta f$ and if it shifts by $-\Delta f$, IF becomes $10.7 - \Delta f$.

2. As an example, the case having IF of 10.75 MHz in FM_L mode is explained. Since IF is to be shifted by +50 kHz, the local oscillator must be shifted by -50 kHz according to paragraph 5) above. Therefore, keeping -1 terminal at "0" to shift -100 kHz, P_{out} terminal should be connected to +50 kHz of TD6102P to shift +50 kHz. By doing this, the local oscillator becomes -100 +50 = -50 kHz and 10.75 MHz is selected as IF.

3. Connections to select one of seven kinds of IF are listed below.

DESIRED IF (MHz) (kHz)		FM_L			FM_U		
		TD6102P		TC9123BP	TD6102P		TC9123BP
FREQUENCY	DEVIATION	+25k	+50k	-1	+25k	+50k	-1
10.775	+75	0		G N D	0	0	V_{DD} or NC
10.750	+50		0	G N D		0	V_{DD} or NC
10.725	+25	0	0	G N D	0		V_{DD} or NC
10.700	0			V_{DD} or NC			V_{DD} or NC
10.675	-25	0		V_{DD} or NC	0	0	G N D
10.650	-50		0	V_{DD} or NC		0	G N D
10.625	-75	0	0	V_{DD} or NC	0		G N D

0 indicates that P_{out} output of TC9123BP should be connected.

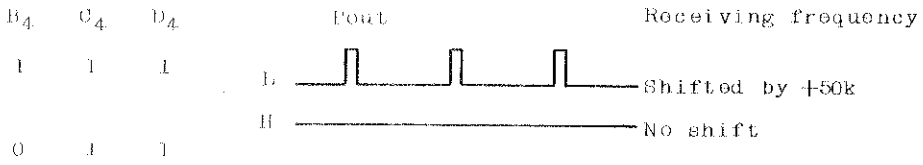
4. This selection of IF is applicable only for 100 kHz spacing of FM_L and FM_U. In the case of 50 kHz spacing for European application which will be described later, P_{out} output of TC9123BP is controlled by control LSI TC9124AP and +50k terminal of TD6102P is utilized for the function to provide 50 kHz spacing, so that IF is fixed to 10.7 MHz.

5. Since the -1 shift operation is not performed even if -1 terminal is connected to "L" level during AM operation, the -1 terminal does not require to be switched according to AM/FM.

APPLICATION FOR FME MODE (50 kHz SPACING)

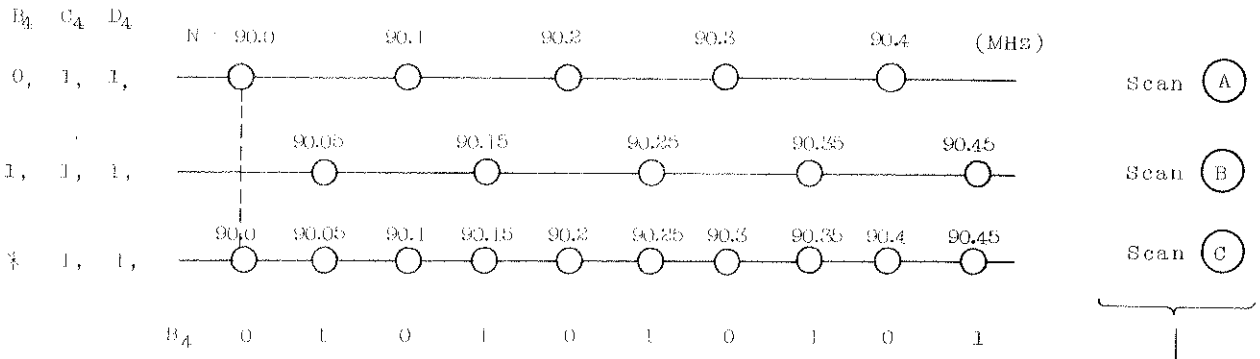
The inter station spacing of FM_L for Japan and FM_U for U.S.A. is 100 kHz, however there are some areas in Europe with 50 kHz spacing. TC9123BP is equipped with FM_E mode to make itself available for the receivers for these areas.

1. The basic operation of TC9123BP in FM_E mode is as follows.
   1) When the receive mode designation data B_4, C_4 and D_4 (B, C and D at the timing of T_4) of TC9123BP are 1, 1 and 1, the frequency division output signal of the programable counter appears at P_{out} terminal.
   2) When B_4, C_4 and D_4 are 0, 1 and 1, the frequency division output at P_{out} terminal stops holding at "H" level.
   3) If the frequency division output of programable counter is connected to +50k terminal of prescaller, the local oscillator frequency is shifted by +50 kHz and the receiving frequency also becomes +50 kHz accordingly. (When the local oscillator frequency is higher.)



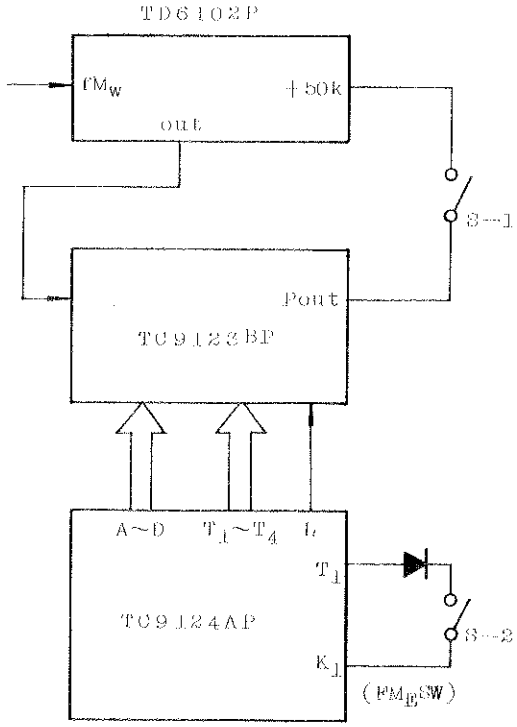
2. If the frequency data is shifted upward fixing B_4, C_4 and D_4 = 0, 1 and 1, therefore, scanning is performed with [multiple of integer of 100 kHz] and if it is shifted upward fixing B_4, C_4 and D_4 = 1, 1 and 1, scanning is performed with [multiple of integer of 100 kHz plus 50 kHz].

3. If B_4 is changed to 0 having N for the frequency data, then B_4 is changed to 1 keeping N for the data, and then B_4 is changed to 0 at the same time as N is incremented by 1, and so forth, the receiving frequency can be scanned with the step of 50 kHz interval.



4. Example of actual circuit with combination of TC9124AP and TD6102P

TC9124AP has the function of controlling FME mode of the above TC9123BP facilitating to realize various operations.



Switches and Scan Modes

	S - 1	S - 2
(A) Scan	OFF	OFF
(B) Scan	ON	OFF
(C) Scan	ON	ON

(Note) For operation of FME mode, the technical material of TC9124AP should also be referred to.

APPLICATION CIRCUIT